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on

Computer Applications

Edited by
I.J.Gabelman

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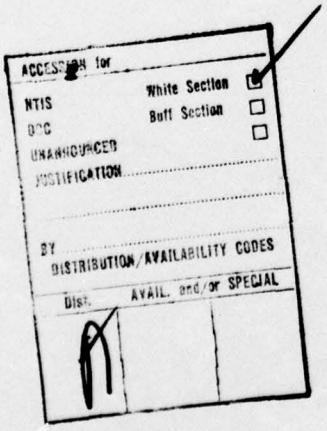
PREFACE

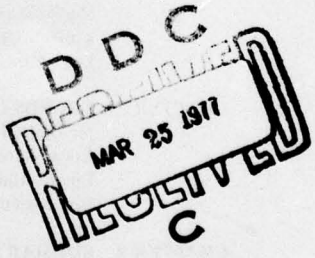
New developments in solid state technology have emerged which make possible significant improvements in computer capability. These improvements allow for wider applicability of data processing equipments in effecting command and control in the NATO military environment.

Solid state technology has decreased by orders of magnitude the volume and power required by computer circuitry and hence has made possible more sophisticated data processing. The technology is now available to construct high level language computers; to control functions in hardware rather than software, to build microprocessors for distributed use in tactical environments; to make available for field use low power, non-mechanical, mass memory systems; to tailor computer architectures to specific applications, and for many other innovative uses.

This report describes the solid state technical developments and assesses the importance of these developments in their application to satisfying NATO military requirements.

Irving J.GABELMAN
Chairman, Editor





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CONTENTS

CHAPTER 1

INTRODUCTION

by

M.C.A.Bijleveld and A.P.DeMinco

Effective control of assigned forces and of air space is deemed necessary for success. Todays tactical warfare is characterized by decentralized activities of highly mobile, dispersed forces operating in a climate filled with technologically complex, and sophisticated equipment. For NATO application, the established wide spread use of infantry, tanks, aircraft, communications, supply systems, etc., together with the newer uses of nuclear weapons, missiles, satellites, and such, define some of the salient aspects of the overall problem. Control of these functions will be accomplished ultimately through a number of miniature general purpose data processors located at surveillance sites, air bases, control posts or centers and the command center. The successful conduct of a tactical operation, the ability to coordinate the many varied aspects of a dynamic tactical situation, depends critically on a combatants capability to handle data efficiently and expeditiously. Techniques applicable to the solution of the multi-faceted problems of tactical data handling have been emerging at an ever increasing rate. Decisive technical developments in semiconductors and computer technology have emerged which offer new possibilities for improvements in computers applicable to the NATO military environment. The chapters that follow describe in detail and give an insight to these new possibilities which could bring advantages in the form of:

- greatly improved overall system integrity,
- greater reliability and maintainability,
- greater capability,
- wider applicability,
- greater flexibility,
- increased speed,
- decreased volume and weight,
- greater ease of use,
- reduction of power dissipation,
- lower costs.

These advantages will be realized if the advantages in computer technology are exploited and timely application to the NATO military environment is made. It is fitting at this stage to attempt to summarize, at least those areas of significance which appear potentially applicable to the NATO area.

In the following presentations some possibilities and difficulties of actual and near future computer systems are related. They intend to give those military systems engineers, who are not quite familiar with all new innovations in the computer field, an insight into what computers could do in military applications. It is appropriate therefore that Chapter 2 begins with a survey of current and future technologies:

In summary, the increase in semiconductor performance during the last 10 years has increased tremendously, e.g.:

- the speed-power product decreased by about a factor of 10;
- the integration increased by a factor of 100;
- the reliability has increased by a factor of 10.

This chapter compares the speed, power consumption, complexity cost and other characteristics and describes as well the most important recent or near future technologies.

The continuous reduction in size and power and the increase in performance and reliability has an important influence upon the packaging of components. In Chapter 3 the different aspects influencing the packaging are mentioned, e.g.: speed, electrical transport, heat transport, reliability, amount of circuits per plug-in assembly, testability, repairability, etc. Likewise, relatively high percentage of packaging trade-offs involve mechanical versus electrical characteristics. It will be noted that mechanical assemblies are subdivided into four levels; different packaging methods in each of these levels are described. Finally some examples of packaging to withstand adverse environments are represented.

The trend of the developments in Large Scale Integration (LSI) and their great impact on computer systems architecture is outlined in Chapter 4. In main memories semiconductors will replace the cores, and cache memories may increase the processing speed if the program structure is well suited and the application is not real-time. Stack memories for interrupt and subroutine handling are common in the present system designs. Content Addressable Memories for virtual addressing (mapping memories) are also slowly finding their way in applications. In the future, discs, magnetic tapes and drums may find strong competitors in Charge Coupled Devices (CCD) and Bubble Memories (BM). The introduction of microprocessors will cause the use of control memories (ROM and PROM) and will assume large scale applications. The microprocessors will create dramatic changes in the architecture of central processors, device controllers and other digital equipment and in the training of digital hardware designers.

In Chapter 5 illustrations of the salient aspects of interfacing are noted, namely a computer with:

- another computer,
- high speed and low speed peripherals,
- analog devices,
- human beings.

The impact of the advances in solid state technologies is also demonstrated.

In Chapter 6, a condensed survey of recent developments in computer communication techniques is given. Special attention is given to certain telephone systems and to generalized methods for computers interacting in networks. Methods, techniques, and subjects of special relevance are outlined. Three specific examples of systems based upon a net of distributed computers for warning, command and control, and communication are briefly outlined. Chapter 9 provides a further expansion in this area citing significant relevance to the Military Tactical Systems and the overall advantages of this technical discipline in computer applications.

Many aspects of digital signal processing are treated in Chapter 7. The need for signal processing in tactical military systems has increased enormously in recent years. All kinds of surveillance, fire control, guidance, communication and other systems require the processing of signals received from sensors. The uses of digital techniques in this area represent a significant advance. Not only do they permit an increase in both computational precision and long term stability but they permit the realization of filters and algorithms which would be awkward or impossible with analog techniques. The significant advances in the simplification of computations by algorithms, such as fast Fourier Transform, in digital processing has enabled these digital techniques to compete much more effectively with analog systems.

In Chapter 8 some trends in airborne computers and some typical airborne applications will be expounded. Still more functions in aerospace are realized by digital computers in places where hydromechanical and analog electronic systems were in common use. It is possible to identify two varieties of applications, that is, real-time applications and data-handling. Both generate their own requirements and can result in very different hardware and software implementations. Typical present day applications are described such as fuel management, engine control, flight control, ECM, AWACS etc. The major difference between airborne and groundbased computers is caused by the stringent physical requirements in the aircraft environment.

The reader will note that during the past few decades, there have been many advances in solid-state technologies and in digital techniques which in turn enables a broad field of application in the computer disciplines. The systems engineer, who is concerned with the NATO military environment, must be cognizant of the proper technologies for ultimate application and implementation for satisfying the requirements of todays tactical warfare. It is hoped that this record of proceedings is some assistance towards that end.

CHAPTER 2

RECENT TECHNOLOGY DEVELOPMENTAL TRENDS

by

R.Boudarel

2.1 INTRODUCTION

Major technological advances have been achieved since the transistor was discovered. These advances have enhanced system electrical and mechanical performances in terms of speed, power-consumption, integration capabilities and reliability.

Integration, moreover, has successively evolved yielding:

SSI: Small Scale Integration
MSI: Medium Scale Integration
LSI: Large Scale Integration

and in the foreseeable future VLSI (Very Large Scale Integration) can be anticipated.

It is interesting to note that between 1965 and 1975, basic component complexity increased more than 100-fold. Similar advances are forecast for the next ten years.

Figure 1 illustrates these technological trends and Figure 2 shows the exponential nature of bipolar technology. Note that the figure of merit, i.e., speed x power, has been reduced by a factor of 10 in 10 years.

Proliferation of basic technologies (refer to Figure 3) has gone hand-in-hand with technological advances; most of these technologies have remained competitive because they offer optimum benefits for specific cases.

The object of this chapter is not to discuss each variant but to:

- introduce terminology,
- present the two main families, i.e., Bipolar and Metal Oxide Semiconductor,
- describe broadly the advances in technology which allow for increased capabilities.

The meaning of main abbreviations used are given on page 18.

2.2 MAIN BASIC TECHNOLOGY

There are two basic integrated circuit (IC) technological families:

Bipolar:

This technology was the first to be employed and began with the discovery of the transistor effect (Figure 4). *Silicon* was shortly accepted as the basic semiconductor used.

Transistors (both p.n.p. and n.p.n.) became the basic element of various electric circuitry which performed elementary combinational logic (AND-OR-NOR-Multiplexer, . . .) and sequential logic (register, flip-flop, . . .) functions.

Circuits are realized from different manufacturing processes (epitaxy, ion implantation, . . .) thereby leading to performance and cost variations.

Metal Oxide Semiconductor (MOS):

The "field effect", more recently discovered, also permits performing elementary functions. Semiconductor and insulator materials (insulator used as a control element) have to be selected for basic components (Figure 5). As mentioned above, electric circuitry design and manufacturing processes naturally yield different types.

	SSI	MSI	LSI	VLSI
Year	1966	1970	1973	1980 ?
Minimum gate delay (ns)	40	6	3	0.5
Chip size (mil)	100	150	250	500
Transistor/chip	50	500	5000	200 000
Random memory (bits/chips)	16	512	2048	64 000
Random logic (gates/chip)	4	50	500	10 000

Figure 1

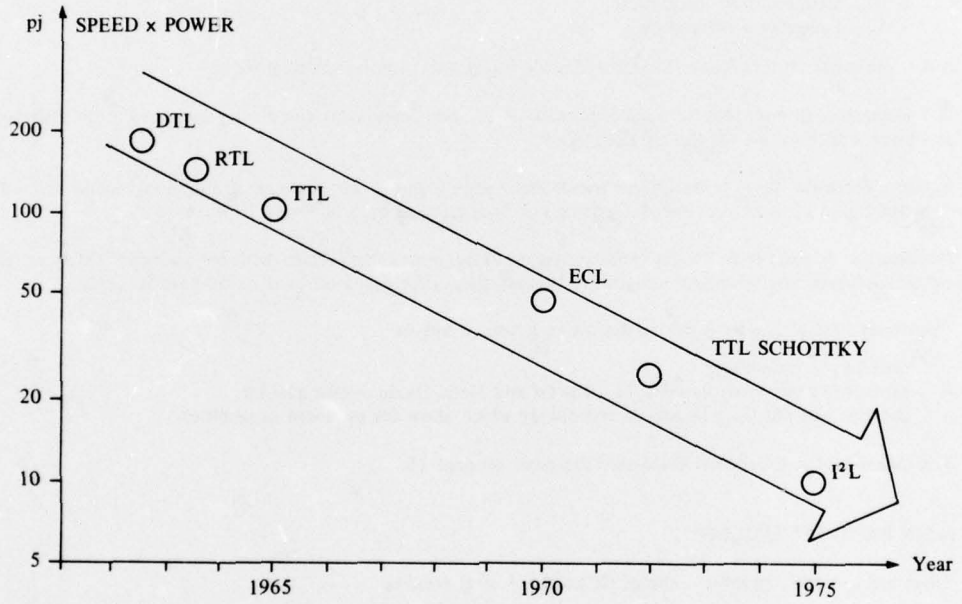


Figure 2

TECHNOLOGIES TREE

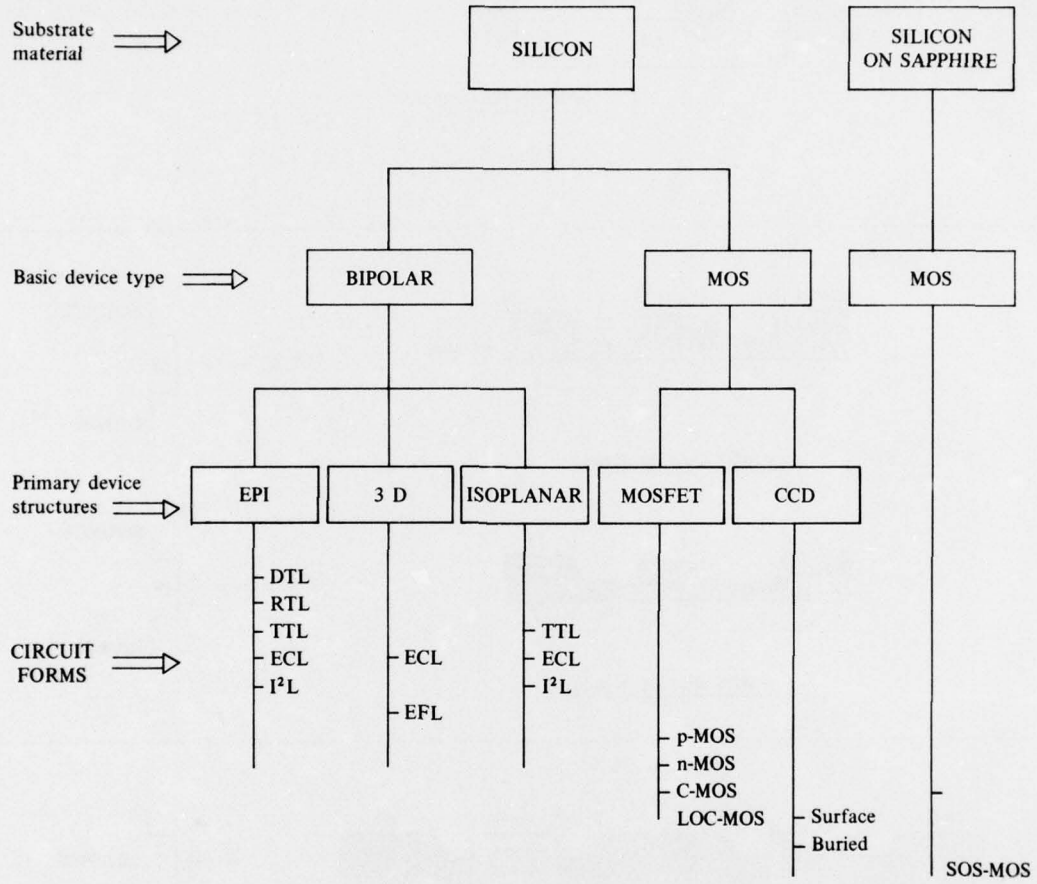
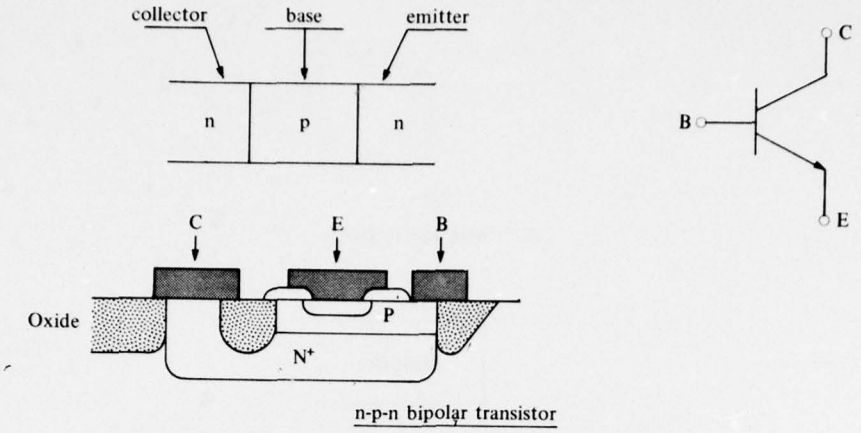
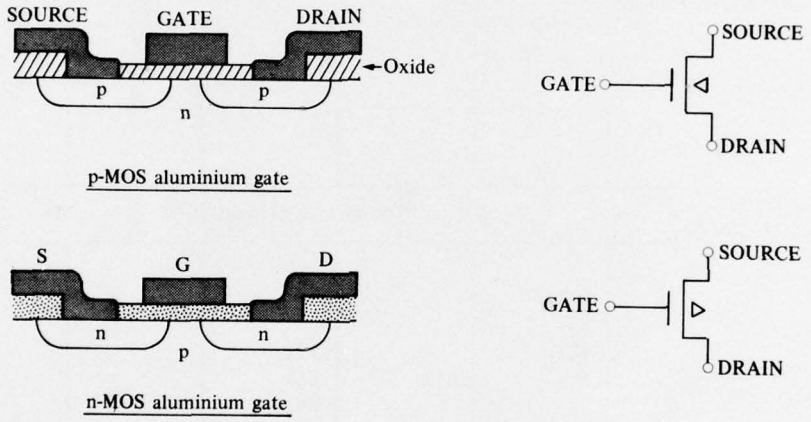


Figure 3



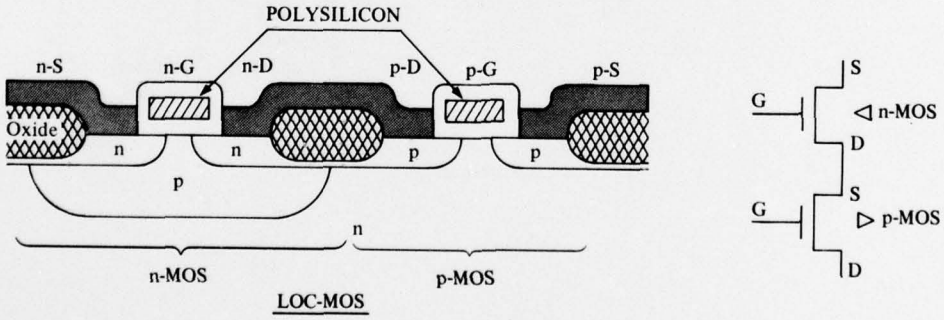
n-p-n bipolar transistor

Figure 4



p-MOS aluminium gate

n-MOS aluminium gate



LOC-MOS

Fig.5 Basic transistor elements (MOS technology)

2.2.1 The Bipolar Family

Although DTL (Diode-Transistor-Logic) and RTL (Resistor-Transistor-Logic) were technologies initially used, TTL (Transistor-Transistor-Logic) shortly became the dominating technology. This was due mainly to its good performances and highly advanced manufacturing processes.

TTL's major feature is its capability of performing basic functions using only elementary transistors (hence its name: Transistor-Transistor Logic) operating in saturated mode.

Technological advances improved speed and reduced power consumption.

2.2.1.1 Faster Speeds

- ECL (Emitter Coupled Logic): (Figure 6) – this fast, unsaturated type technology is difficult to use because short wire-leads are mandatory.
- TTL-S (Transistor-Transistor-Logic-Schottky): (Figure 7) – Schottky effect diodes are used to reduce recovery times of charges stored under saturated operating conditions.

Faster speeds are paid for with higher power consumption.

2.2.1.2 Reduced Power Consumption

- TTL-LP (Transistor-Transistor-Logic Low-Power): Reduced power consumption paid for here by slower speeds; as a result, this technology is limited to applications where power consumption is the main criterion.
- TTL-LS (TTL-Low power-Schottky): this extremely promising technology combines TTL Schottky and TTL Low Power advantages. Standard TTL compatibility and advanced industrial stage of development should enhance its production.

2.2.1.3 Foreseeable Industrially Produced Technologies

Main manufacturers have been announcing new production lines but which of the laboratory species will be industrially produced is still difficult to determine.

- I^2L (Integrated Injection Logic) (Figure 8)

  This technology leads to production of elementary logic gates which are composed of complementary pairs of transistors. Being current driven, I^2L enables logic operations to be directly realized through output wiring. This results in a reduction in the number of elementary transistors required and in power consumption while performances comparable to TTL are still retained. A major R and D effort is being made on this technology

- EFL – (Emitter Follower Logic (Figure 9))

  This technology relies on three-fold diffusion to insure a high degree of integration with fast speeds. *This technology is at the laboratory stage.*

2.2.2 MOS Family

Metal Oxide Semiconductors (MOS) are employed in a wide variety of components. In particular:

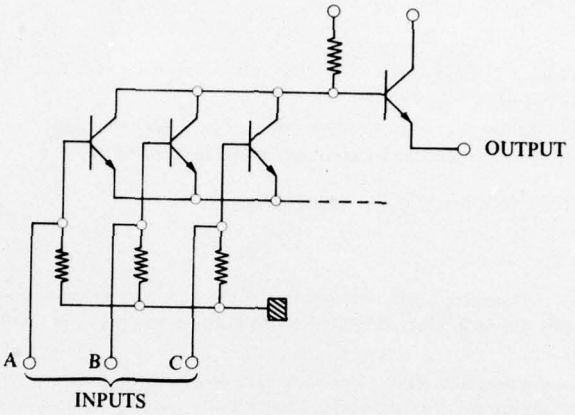
(a) channel type: p (positive) or n (negative)

(b) class: depending on electric operation (see Figure 10)
- I – Enhancement (activated: current increase)
- II – Depletion (activated: current decrease)
- III – Complementary (CMOS) combination of I and II.

(c) technological family
- Aluminium gate,
- Silicon gate,
- Silicon on insulated substrate.

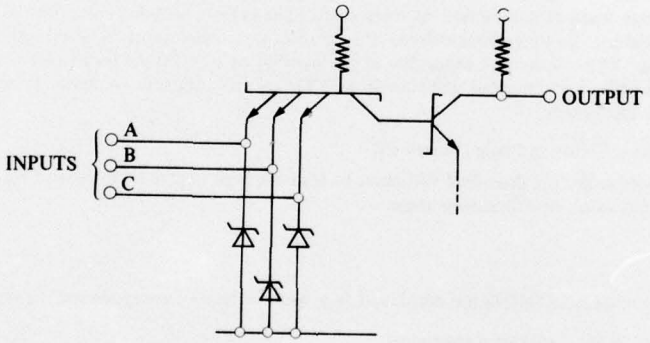
When (a), (b) and (c) features are combined, up to 15 different basic MOS devices are obtainable.

Other parameters such as silicon crystalline orientation, ion implantation, etc. may be incorporated in this classification.



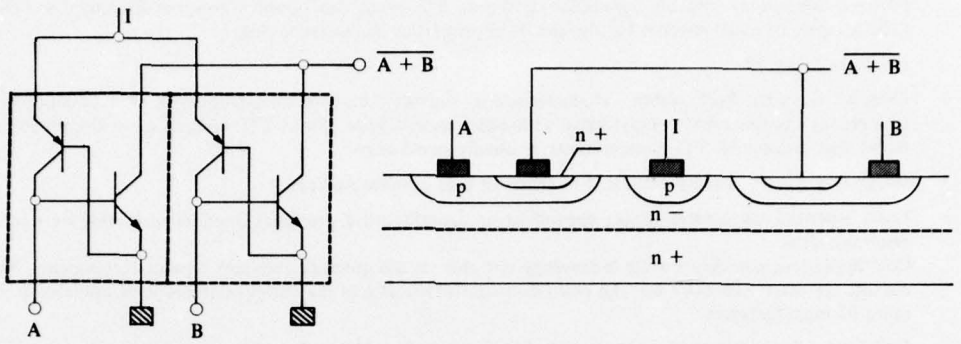
ECL NOR

Figure 6



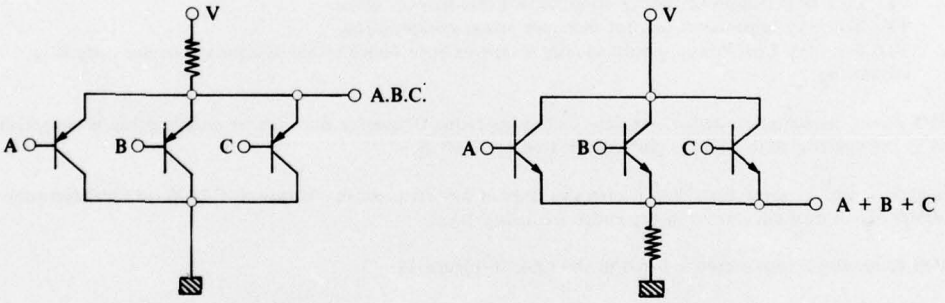
TTL SCHOTTKY NAND GATE

Figure 7



I^2L basic element

Figure 8



3D/EFL WIRED AND and WIRED OR

Figure 9

2.3 TECHNOLOGY COMPARISON

Technology performances are characterized by numerous parameters. Basic criteria vary with the type of application, and trade-offs will necessarily arise. Main parameters are as follows:

- *Speed*: expressed in propagation time or maximum operating frequency. This parameter may be evaluated at the elementary transistor, elementary circuit (gate), or whole logic circuit level.
- *Power Consumption*: usually dependent on speed. The product of speed x power is often used and constitutes a figure of merit specific for the electrical properties of the technology.
- *Fan-in and Fan-out*
- *Complex Circuitry Realizability*: characterized by fan-out (i.e., maximum number of circuits connectable to a circuit's output) and compatibility with other technologies. Since TTL technology is the predominant technology employed, TTL compatibility is usually mandatory.
- *Integration Level*: usually expressed in terms of gate number/package.
- *Cost*: essential economical factor; dependent on manufacturing processes (number of masks, etc.) and resultant yield.
  Cost dependent not only on the technology but also on the quantity sold and type of component. New circuits are often expensive but the price decreases drastically as the component becomes available from more IC manufacturers.
- *Reliability*: basic factor for military and airborne systems. Although technology plays a somewhat significant role in reliability, manufacturing methods and quality control have major impact on results.

  It should be noted that usually only old, well-established technologies have accurate and realistic numerical results. For example, for TTL, MSI is well known but LSI can only be estimated.

2.3.1 Speed Versus Power Consumption

Figure 11 indicates typical values on propagation times and power consumption/gate.

It is interesting to note that starting from the initial relationships:

- propagation time ECL < TTL < MOS
- power consumption ECL > TTL > MOS

- TTL Low Power improves power consumption but reduces speed,
- TTL Schottky improves speed but increases power consumption,
- TTL Schottky Low Power simultaneously improves both factors; this obviously indicates why it is interesting.

MOS power consumption depends mainly on the operating frequency since power consumption is appreciably lowered in the standby state. This is particularly true for C-MOS.

Figures 12 and 13 show that MOS is effective only at low frequencies. However, C-MOS on insulated substrates offers operational advantages in the entire frequency band.

MOS technological advances are listed in the table in Figure 14.

2.3.2 Integration – Yield – Cost Comparison

Integration – Yield – Cost factors are usually interrelated.

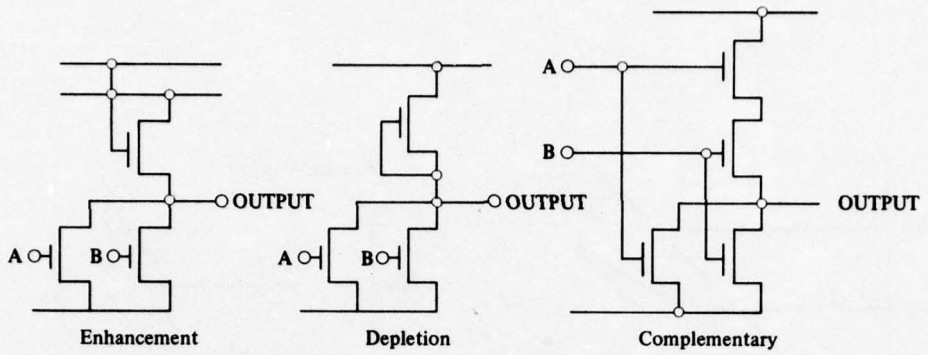
Possible heat dissipation per package determines the silicon chip size. However, the yield is related to the elementary dimensions of the basic circuit. Indeed, resultant trade-off varies with the technology type and it depends on the manufacturing process: number of masks, ion implantation, . . .; insulation of the various basic elements is also an important factor.

Generally, MOS technologies lead to higher integration than TTLs because the basic circuit (elementary gate) is smaller and its corresponding power consumption as well.

However, new TTL-LS and I^2L technologies should permit obtaining results comparable to MOS.

The table in Figure 15 makes a comparison between basic element cost and surface occupied by MOS technologies.

The table in Figure 16 makes a comparison between surface and manufacturing parameters for basic technologies.



MOS FAMILY

Figure 10

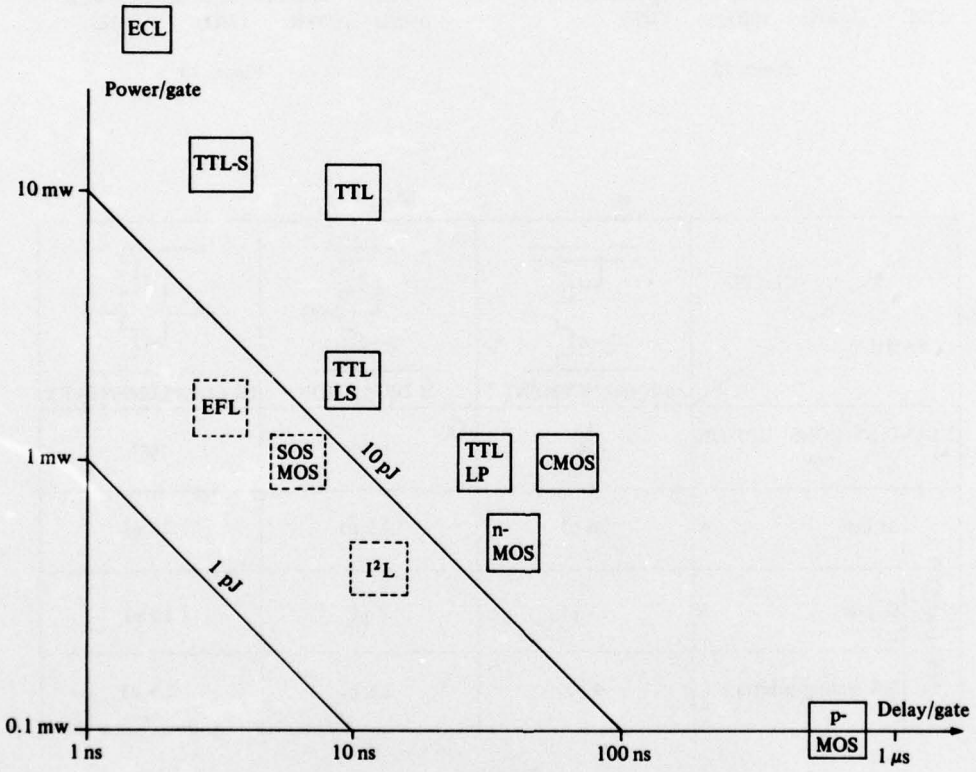


Figure 11

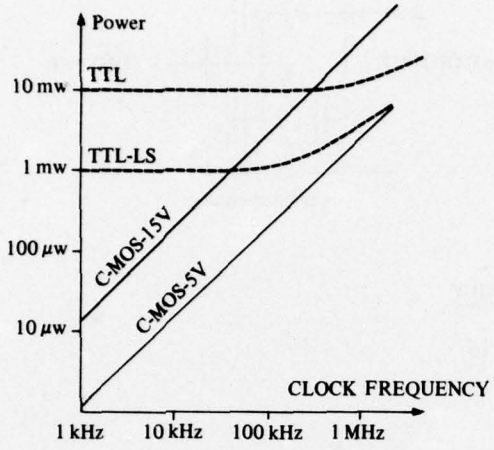


Figure 12

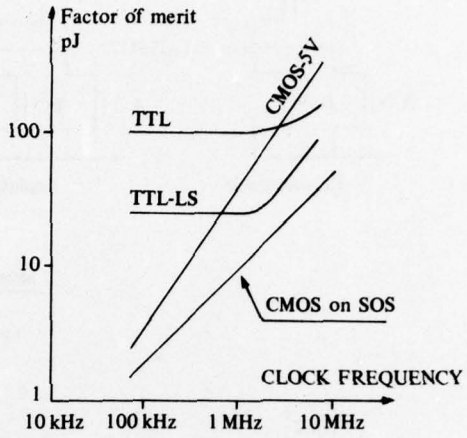


Figure 13

FAMILY / CLASS		I ENHANCEMENT	II DEPLETION	III COMPLEMENTARY
STAND BY CONSUMPTION mw		1	1/20	10^{-5}
SPEED x POWER	Al gate A	20 pJ	13.5 pJ	26 pJ
	Si gate B	13 pJ	7 pJ	10 pJ
	Si/isolating substrate C	4 pJ	2.8 pJ	2.8 pJ

Figure 14

FAMILY \ CLASS	I	II	III
Al gate A	Reference/Reference	1.2/	1.5/3
Si gate B	1.3/0.5	1.5/0.7	1.8/2
Si/isolating substrate C	1.1/0.5	1.3/0.7	1.6/1

PRICE // ELEMENTARY SURFACE For MOS technology

Figure 15

TECHNOLOGY	NORMALIZE GATE-AREA	NUMBER OF DIFFUSIONS	NUMBER OF PHOTORESIST STEPS
TTL	1	4	6
TTL-Schottky	1	4	6
TTL-LS	1	5	7
ECL	0.9	5	7
n-MOS	0.3	1	6
C-MOS	0.55	3	7
I^2L	0.25	2	4
EFL	0.42	3	5

Figure 16

These factors all impact on the manufacturing potentialities of the technologies. However, final component price depends on many other factors, including IC manufacturer's sales policies, and international market evolution. It is normal for the price of a new integrated circuit to vary by a factor of 10, and, especially, for microprocessors.

2.3.3 Conclusion

In the early 1970s, the relative merits of MOS-TTL-ECL basic technologies were clearly outlined.

These advances enabled:

- improving technologies in terms of:
  - speed
  - power consumption
  - integration
- introducing new solutions: I^2L-EFL.

The situation has become complicated and the selection of technologies now depends heavily on each application's requirements.

2.4 ELEMENTARY CIRCUITRY APPLICABILITY

Basic circuit complexity is directly linked to the extent of the technology's integration and the question of heat dissipation; however, output pin availability on the package is the most critical factor.

This mechanical aspect will be discussed to show how it often reduces integration possibilities well below technological limits.

2.4.1 Logic Circuits

Elementary logic circuits realization (NAND with n imputs, multiplexers with n inputs, flip-flops, . . .) is limited directly by the number of package pins.

Integration calls for complex circuits which tend to arouse general interest. Such circuitry comprises:

- Arithmetic and Logic Unit (4 bits): ALU
- Programmable Logical Array: PLA
- Multiplier (4 x 2)
- Decoders.

2.4.2 Microprocessors

The ratio of gates-to-output-points for such a logic function is extremely high and favors a high level of integration. Technological possibilities as opposed to those indicated in paragraph 2.4.1, still constitute main limits.

An entire minicomputer (ALU + Memory + Interface) within a single IC-package may be built today only in the laboratory; marketed systems are subdivided into elementary subassemblies.

There are two types of subdivisions:

- "bit slicing": all data paths are sliced in parallel and the desired format is obtained by physically juxtapositioning the elements.
- "n bit microprocessor": where n depends on the extent of integration (4–8–16) Data with longer formats are sequentially processed (time slicing) in n fold lengths.

When TTL-LS or I^2L technologies are used, the first subdivision ("bit slicing") provides high performances and proposed components insure greater system architectural flexibility (e.g., INTEL 3000 in TTL-LS). Most circuits have a 4 bit/slice structure. Hence, the number of bits for the final microprocessor may be selected (16-bits calls for 4 ICs).

The second subdivision (n bit microprocessor) is aimed more at integration than performance and imposes a less flexible system architecture. Highly integrated MOS technology is the most widely used. (e.g., MOTOROLA 6800 in MOS-n). Most microprocessors of this type are 8-bit, although 12- and even 16-bits are already under development.

2.4.3 Memories

Semiconductors permit construction of a wide range of memory types: ROM (Read-Only Memories), Rewrite Memories (Mostly Read), RAM (Random Access Memories) with cycle times between tens to some hundreds of nanoseconds.

(a) *RAM (Random Access Memory)*

Technology is selected according to the speed required: MOS (150 to 650 nanosec.) – TTL (50 to 150 nanosec.) – ECL (less than 50 nanosec.).

For MOS, static memories must be distinguished from dynamic memories; dynamic memories use the special MOS feature of storing data in parasitic capacitors which, in turn, simplify memory cell electric circuitry (see Figure 17); on the other hand, data saving requires cyclic refreshment (a period of a few millisec.).

Figure 18 indicates speed and bit number per package for the three basic technologies with MOS used as a reference. In 1975, standard MOS technology speeds are approximately 500 nanoseconds for a 4 Kbit package.

By the late 1970s, 16 Kbit packages should be mass-producible.

(b) *Permanent Memories*

These memories are becoming more widely used as an indispensable microprocessor complement.

Storage is either executed with an interconnection mask (ROM) or written electrically (PROM); PROM utilization offers the user greater flexibility.

The write process (current intensity and duration) interferes directly with memory reliability.

As mentioned above, Figure 18 shows permanent memory performances. Roughly speaking, a PROM (Programmable Read Only Memory) is twice as fast and contains four times as many bits as an equivalent RAM (Random Access Memory).

(c) *Rewrite Memories*

The major disadvantage of semiconductors, as compared to core memories, is the semiconductor's volatile (RAM) or permanent (ROM, PROM) nature. Now, many applications require program or parameter changes plus data-save security until the next change, and, at the same time, must be safe from power supply fluctuations.

Two currently available technologies satisfy such requirements:

- E-PROM: Erasable memory using ultraviolet radiation,
- MNOS: MOS memory with dual-gate insulator.

E-PROM is at the manufacturing stage; MNOS, although more flexible in use than E-PROM, is still in the preproduction stage with only a limited degree of integration.

These two technologies still raise many problems in terms of data storage times, especially for data storage under severe environmental conditions.

(d) *Associative Memories*

Associative memory advantages have been emphasized for quite some time. Semiconductors may be used to build associative memories, but associative memory costs are still 1.2 to 1.5 times higher than RAM equivalents. Only laboratory prototypes are currently available.

2.5 SEMICONDUCTOR VERSUS OTHER TECHNOLOGIES

2.5.1 Processing

The semiconductor is a universal solution for digital data processing; in the special case of image processing, the optical computer processes the image with a high degree of parallelism (2 dimensional transformation). However, microprocessor manufacturing cost reductions should enable the realization of array and associative memory structures at competitive prices.

2.5.2 Main Memory

Magnetic memories are still the most commonly used. Core memory manufacturers do not foresee a reduction in production before 1980. Several reasons can be given to explain this:

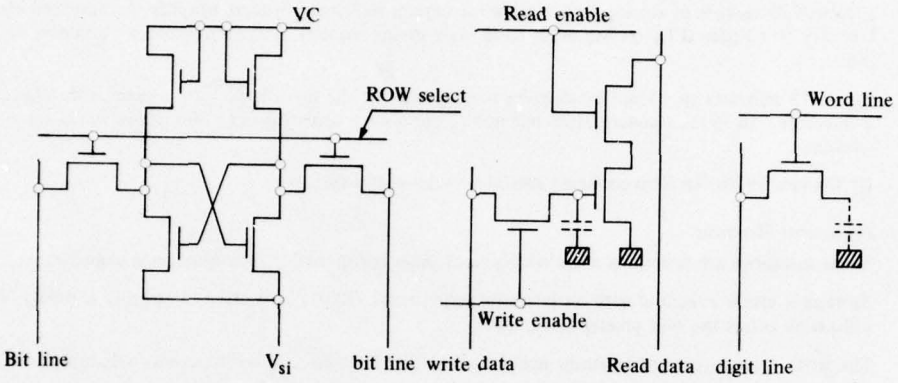


Figure 17

		ECL/MOS	TTL/MOS	MOS
RAM	Speed	8	4	Reference value
	Nb bit/package	1/16	1/4	
PROM	Speed	16	8	1
	Nb bit/package	1/8	1	2

Figure 18

- industrial advantages: considerable investments (research, development, production) have enabled the magnetic core to keep pace with semiconductor advances in terms of price, speed, and compactness.

For large-capacity memories, magnetic core price per bit is still competitive and when a fast semiconductor cache memory is used, apparent speed approaches that of the semiconductor's.

- operational advantages:
  - permanent data availability with non-destructive read for plated-wire-memories,
  - better immunity against environment,
  - power consumption increases (reliability decreases) slower with memory capacity than in the case of a semiconductor where they are proportional. Consequently, the magnetic core is more favorable for large stores.

2.5.3 Mass Memories

Magnetic memories (disks) recording densities (linear and transversal) are constantly being increased. Data capacity for equivalent mechanisms is doubling every 3 years. As a result, other technologies can hardly compete with mass memories in terms of price per bit.

Major disk handicap arises from its access time due to mechanical limitations (rotational speed); average times range from 10 msec (fixed head) to 70 msec (mobile arm).

Magnetic technologies (without mechanical movement) are being studied; these include bubble or "domain displacement" memories.

In the semiconductor field, dynamic shift memories (CCD transistor) provide the highest extent of integration.

In both cases, data must be stored in shift registers so maximum data density may be attained. This obviously entails access times proportional to elementary register lengths. Several parallel-level organizations have been proposed to improve apparent access times.

Table (Figure 19) summarizes foreseeable developments. It is possible to forecast from this table that in 1980:

- the disk will still be cheaper,
- the CCD will attain faster access times, but is volatile.

	YEAR	MAGNETIC DISK	BUBBLE MEMORIES	HOLOGRAPHY MEMORIES	CCD MEMORIES
Storage density (bit/mm²)	1975	$2.5 \cdot 10^3$	$10^3 - 10^4$	10^4	10^3
	1980	$2 \cdot 10^4$	10^5	10^5	$2 \cdot 10^4$
Module capacity (bit)	1975	$2 \cdot 10^9$			
	1980	$2 \cdot 10^{10}$	10^9	10^{10}	10^9
Access time μs	1975	40 000	500	10 – 100	10 – 100
	1980	25 000	100	10 – 100	1 – 10
Price/bit	1975	$7 \cdot 10^{-5}$			
	1980	$5 \cdot 10^{-6}$	$10^{-3} - 10^{-4}$	$10^{-3} - 10^{-4}$	$10^{-3} - 10^{-4}$
Price x access time	1980	0.125	0.1 – 0.01	0.01	0.001
Technology available		yes	no ?	no	no
Non volatility		yes	yes	yes	no

Mass memory technologies

Figure 19

CHAPTER 2 ABBREVIATIONS

ALU	Arithmetic and Logical Unit
CCD	Charge Coupled Device
CMOS	Complementary MOS
DTL	Diode Transistor Logic
DTPL	Domain Transition Propagation Logic
ECL	Emitter Coupler Logic
EFL	Emitter Follower Logic
EPI	Epitaxial
3D	Three Diffusion
E-PROM	ReProgrammable Read Only Memory
FET	Field Effect Transistor
IC	Integrated Circuit
I^2L	Integrated Injection Logic
LSI	Large Scale Integration
LOCMOS	Local Oxidation CMOS
MOS	Metal Oxide Semi-conductor
MSI	Medium Scale Integration
PLA	Programmable Logical Array
PROM	Programmable Read Only Memory
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Resistor Transistor Logic
SOS	Silicon Transistor Sapphire
SSI	Small Scale Integration
TTL	Transistor Transistor Logic
TTL-LP	TTL-Low Power
TTL-LS	TTL-Low Power-Schottky
TTL-S	TTL-Schottky
VLSI	Very Large Scale Integration

CHAPTER 3

PACKAGING AND ASSEMBLY TECHNIQUES

by

J.McCormick

3.1 INTRODUCTION

For computers, the packaging goal is to mount and interconnect the electronic components into a suitable assembly. Suitability encompasses many factors including cost, performance, physical characteristics, and practicality. Selecting the best trade-offs among these factors is essential to good packaging design. The assembly technique chosen for a computer design is usually determined by the speed requirements, intended application, and the circuit design. This is especially true of digital systems in which the large component count may lead to excessive size unless close attention is given to packaging and assembly. At best, the volume ratio of the packing interconnection, heat sinking, and mechanical support material to the active semiconductor device material is orders of magnitude greater.

Computers are referred to as belonging to generations that have been defined by their types of active elements. The generations, as defined, tend to segregate computers conveniently for packaging considerations. Four generations have been defined as follows: first generation computers consisting of vacuum tube circuits, second generation computers that are characterized by transistor circuitry, third generation computers that have been constructed with integrated circuits (ICs), and fourth generation computers which are constructed using large-scale integration (LSI).

The evolution of computers has been marked by a continual reduction in size and power, concurrent with demands for increased speed and reliability.

A typical product program for a digital computer encompasses three years for development and a market life of five years or more. The complexity of development, manufacture, and application of such computers, particularly in large-scale systems, tends to discourage early model change on the part of both supplier and user. The packaging engineer, as a result, is faced with the dilemma of committing, for a long period of time, designs chosen from a rapidly changing technology. Selection of circuit and packaging may be required some two years before the equipment first reaches the user. Automated processes for design, fabrication, and testing of computer hardware decrease the interval between technique selection and market introduction. But even if this portion of the development time is reduced substantially, most of the utilization still occurs several years after packaging selection. One must select, from among the latest electronic packaging techniques in the laboratory, those that will best survive this utilization.

Most computer packaging engineers agree that their techniques are two to five years behind state-of-the-art techniques. The packaging engineer cannot afford to incorporate "technology fads"; there must be sound technical and economic reasons for the choice. However, trends in packaging resulting from circuit technology advances must be recognized by the packaging engineer if he would optimize his design to accommodate future generations of computers.

3.2 ELECTRICAL AND MECHANICAL PACKAGE DESIGN CONSIDERATIONS

Before design starts, trade-offs are considered sometimes unconsciously, sometimes more formally. A relatively high percentage of trade-offs involve mechanical versus electrical characteristics. Many of these are discussed in Table 1 and should be considered when making the preliminary trade-offs. Active semiconductor devices (integrated circuits) are usually packaged by the manufacturer in hermetically sealed glass or ceramic flat packages or dual in-line packages which are approved for military use. However, less expensive, non-reliable, non-hermetic dual in-line packages using plastic encapsulation in lieu of a hermetic seal are sometimes used in commercial equipment for noncritical applications.

Selection of circuit groupings and plug-in levels has a great effect on interconnecting wiring. In general, the greater the number of circuits per plug-in assembly, the greater the number of output pins required. However, it is not a linear factor, and eventually the number of pins required decreases.

TABLE 1

Electrical versus Mechanical Trade-offs for Various Packaging Techniques

Technique	*Electrical characteristics*	*Mechanical characteristics*
Dual In-Line integrated circuits on printed-circuit boards. (Dual In-Line-A component which terminates in two straight rows of pins or lead wires)	Average interconnection propagation delay Good isolation possible High-impedance circuits marginal Mutual capacitance and cross-talk between lines likely Difficult to shield effectively	Good trade-offs in size fairly small but utilizes standard printed-circuit techniques Can be flow-soldered in large quantities Individual units can be replaced Multilayer boards required for maximum density Compatible with conventional components Assembly utilized standard printed-circuit techniques Good connection but poor heat conduction characteristics
Flat-pack integrated circuits on printed circuit boards	Average interconnection propagation delay Good isolation possible Crosstalk on boards likely High-impedance circuits marginal Difficult to shield effectively	Several fastening methods available Two-dimensional fastening is much simpler than stacked flat packs Small quantities require printed-circuit artwork Spacing may be dictated by connectors Individual flat packs can be replaced Not compatible with three-dimensional parts Heat can be conducted away easily
Hybrid Integrated circuit packages	Isolation between circuits possible Short leads-minimum propagation delay Resistor and capacitor values limited Not applicable to high power or high voltage	Use standards circuits – no complex masks Interconnections reduced but usually made point by point High-cost throwaway unit
LSI (Large Scale Integrated Packages)		
A. Bi-polar devices	Fast circuit and interconnection propagation speeds Isolation between circuits difficult Active devices easy to make Changes impossible Large-value resistors and capacitors impossible Not applicable to high power or high voltage	Interconnections built in very small size Long development time for new masks Costly for small quantities High-cost throwaway unit
B. MOS (metal)	Slow circuit propagation speeds Parameters unstable Large fan-out No passive components necessary	Small size Heat dissipation difficult Interconnection large with respect to device Low cost on basis of small area Single diffusion process

Reliability of a system is difficult to evaluate properly. All too often, joint reliabilities are overlooked. Each soldered joint, each sliding contact, each welded joint, and any other method of interconnecting detracts to some extent from system reliability. Given the same set of conditions, fewer joints mean better system reliability. Total number of pins is not the same as total number of joints. Each "pin" may contain several joints – for example, a crimp, a sliding contact, and two solder joints in series.

Large systems should be built so that interim testing of subassemblies is possible. Critical signals should be brought out to a position where they can be analyzed. Test capabilities are easy to overlook, but necessary. Testing

may be done on many levels. Where automatic testing equipment is available, 100 percent testing of components may be practical. Sometimes subassemblies can be repaired less expensively than all components can be tested. Often, rework is impossible. Subassemblies which are embedded in plastic are commonly thrown away if they do not work properly. Molded subassemblies are generally tested before embedment to detect bad components, incorrect connections, or poor joints. They must be structurally sound to avoid damage during premold testing. Premold and postmold test results may be compared to ascertain changes due to molding.

Providing test points is a compromise to optimum packaging design. Do not arbitrarily bring out leads which would normally be buried deeply inside a subassembly; consider the effect on system performance. Additional electrical problems are nearly always discovered when test points are added as an afterthought. Sophisticated systems require many test points to locate failures. Complicated fault-isolation circuits may be necessary, and the packaging design is correspondingly compromised. Design of the fault-isolation circuits should relate to replaceable units and coincide with packaging design. Built-in test circuits may be used to test a system in place. Initiation of the built-in test circuit cycles a series of tests and presents some type of intelligence indication that the equipment is working properly. Again, packaging design is compromised by the addition of what may be fairly complicated circuitry.

Practically impossible repair situations are sometimes built into equipment simply because repairability was not considered. Not only should repair be possible but repair time should be consistent with system usage.

Standardization makes a system easier to build, easier to stock parts for, and easier to test, replace, and repair. On the other hand, standardization may lead to more complex wiring, and to some degree it also limits flexibility in design. Point-to-point wiring may be used to reduce pick-up, but systems built this way tend to be large in size. Lead length may limit signal propagation time and, therefore, operational speed. Board cost, lack of flexibility, and long design time are disadvantages of the specific-function circuit grouping approach, but simplified wiring, smaller size, and electrical advantages of the specific-function grouping may outweigh the disadvantages. Each system must be evaluated on its own merit.

Some of the effects circuit grouping can have on electrical characteristics are listed in Table 2 and indicate what the packaging engineer should consider. The effect varies with the packaging technique. Summing resistors of a high-impedance circuit, for instance, will have parallel impedance paths across the surface of the glass-epoxy board. If the same components are embedded in epoxy, the parallel paths may be beyond acceptable levels. High-impedance circuits should be grouped so that they can be dealt with much more effectively.

TABLE 2

Effects of Packaging on Electrical Characteristics

Packaging Technique	*Possible Effect*
Tight packaging	Effective isolation impossible
Long leads	Increase propagation time
Parallel wires	Crosstalk
Low-level signal next to power line	Pickup on signal line
Parallel lines on printed-circuit board (same or opposite sides)	Mutual capacitance: crosstalk
High-impedance circuits on printed circuits	High-impedance shorts across the surface in humidity
Embedding of soldered or welded modules	Circuit changes caused by pressure and dielectric characteristics
Soldering components by hand	Component changes caused by heat
Grounding power and signals together	Signal interference through ground
Large embedded subassemblies; leads from internal stages not brought out	Impossible to test once molded
No stress relief loop in wires or components	Intermittents and opens
No heat sinking on high-wattage components	Component failure
Sharp corners on high-voltage lead terminations	Corona
Basing subassembly design on overall power dissipation	Hot spots-component failure
Space not allocated for test points	Fault isolation very difficult
Plug-in of simple subassemblies	Many joint resistances in series

The technique for the removal of heat from an assembly must be carefully determined. Forced air cooling is usually considered to be the most effective method, with either the cooling air being passed directly over the components, or through heat exchangers to which the best heat producing components are attached.

3.3 MECHANICAL ASSEMBLY LEVELS

Mechanical Assembly Levels may be used in categorizing the significant differences associated with different levels of mechanical assembly used within a package, or Package Element.

Mechanical Assembly Levels are used primarily to provide a format for collecting, correlating and comparing data on package designs. The physical size and the number of assembly levels used vary widely in the types of electronic equipment with which microelectronic circuits may be used. Consequently, configurations which have been developed are not directly comparable as total packages. However, if several total packages are divided into parts by Mechanical Assembly Level, the design methods used within a particular level will have a significant degree of commonality. Data from sources using all or partial combinations of these levels can then be correlated by individual level for analysis and comparison. Mechanical Assembly Levels are defined in Table 3.

TABLE 3

Mechanical Assembly Levels

Level	
1	The lowest level of packaging an electronic device or circuit, commonly referred to as the "component level". Example: A discrete resistor or an integrated circuit.
2	The second level of assembly generally consisting of components grouped on a card, chassis, or module. Example: Circuit cards, or flat pack modules.
3	The third level of assembly consisting of groups of Level 2 assemblies. Example: Card mounted modules.

1. *Level One, The Integrated Circuit or Array*

A suitable package for an integrated circuit device must:

(a) Be strong enough mechanically to withstand stresses during assembly, system packaging and use.

(b) Be small and shaped so as to permit stacking or some other compact aggregation.

(c) Provide easily established and reliable electrical connections from the inside circuit to the outside environment.

(d) Hold to a minimum parasitic inductance and capacitance, in spite of the high packaging density of the conductors enforced by the small overall dimensions.

(e) Have a thermal resistance as low as possible from the circuit to its outer environment.

(f) Maintain an interior environment which is stable and congenial to the circuit.

(g) Shield the circuit from electro-magnetic fields.

The geometries of the various integrated-circuit packages have been standarized by the manufacturers through the Electronic Industries Association (EAI). Thus, the TO designations are assigned by the EAI after full coordination between the manufacturer and user.

2. *Level Two*

(a) Printed Wiring: Printed wiring, as a general class, can offer satisfactory performance in varying degrees, depending upon the type of printed-wiring plane used. Wiring accuracy may be substantially enhanced by using computer-generated wiring lists and automated artwork production. Reliability is probably the best of any wiring system employed today. In addition, the rigid-printed wiring system has the potential of extreme miniaturization and is naturally amenable to mass production not only in the printed-wiring-plane manufacturing phase, but also if a flow soldering technique is used, in assembly of components.

Design flexibility is relatively good before a design is committed; thereafter, of course, it requires a change in artwork, and changes are not easy to make. In the same manner, printed-wiring boards are not easy to change after their fabrication is completed. Advantages and disadvantages of rigid printed wiring are covered in Table 4.

TABLE 4

Advantages and Disadvantages of Printed-Wiring

Advantages	*Disadvantages*
1. Lowest cost for large-quantity production	1. High cost for small-quantity production
2. Good weight and space minimization	2. High tooling and artwork costs
3. Provides structural support for components, versatility in package design	3. Difficult to repair
4. Rapid installation, can be mass-soldered	4. Design must be fixed to be feasible on a cost basis
5. Can provide voltage and ground busses	5. Reliability of interlayer connection varies with fabrication technique
6. Can provide transmission-line capability	

Single-sided Boards: The simplest and most common of all printed-wiring media, this configuration also has the lowest pin density. Components may be surfacemounted but are more often mounted through holes (usually punched) and mass soldered to the wiring. It is the most reliable and also the most easily maintained of all board types.

Double-sided Boards: The double-sided board must have some interside connection method, resulting in a loss of reliability to some extent. It provides more density capability than the single-sided board; however, it is two to six times more costly. Although this board permits the attachment of components to both sides of the board, attachment is made to one side only if flow soldering is to be used.

Multilayer Boards: The ultimate in printed-wiring density, this technique is required where circuitry requirements dictate a high interconnection density. Depending upon particular application involved, space savings over single-sided and double-sided printed circuitry of 15 percent to 70 percent can be realized. However, contrasted with comparable double-sided board, the cost can be expected to increase at 25 percent plus 10 to 12 percent per additional layer.

Multilayer printed wiring is a natural extension of double-sided printed wiring; the density and crossover capability were not available and additional layers of wiring were laminated to provide a functional monolithic wiring plane. In general, multilayer printed-wiring boards may reduce space and weight, provide for greater density of plug-in components, and assure enhanced reliability and cost savings resulting from closely controlled mass processing. Their individual constructional features make them particularly adaptable for some jobs and unsuitable for others.

(b) Plug-in Solderless Wrap Panels: An alternate to printed wiring is the solderless wrap approach, which allows dual in-line devices to be plugged into a board. This technique is advantageous during design. New integrated circuits are plugged into the socket patterns, and wiring changes are made with hand wire wrapping tools. This eliminates waiting for new layouts on printed circuit boards. It has the disadvantages of increased size and decreased reliability.

(c) Multiwire Boards: The multiwire board appears very similar to a printed circuit. Components can be hand- or machine-inserted, and the board can be soldered with the hand iron or wave-soldering method. Repair techniques and component replacement procedures are almost identical to those used for printed circuits. However, the conductors are not printed and etched copper but, instead, are actually insulated copper wire.

The wire is placed on the board by a numerically controlled machine which uses ultrasonic energy to embed the wire in a thin, thermoplastic adhesive on the surface of the base substrate. Connections to the wires are made by selectively drilling a wired board, chemically cleaning the holes to expose the stub ends of wires which have been drilled through, and depositing electroless copper to form component holes and, at the same time, make connections to the wire ends.

Multiwire boards incorporate a printed circuit pattern on the base substrate for such features as fingers for edge connectors and power busses. Recent trends have been toward large areas of copper for power and ground planes to give improved high frequency electrical characteristics. In a configuration with a ground plane on one side of the base substrate, a power plane on the other side, and planes covered with dense wiring, a multiwire board gives the equivalent interconnection density of a six or seven layer multilayer board.

The widest use of multilayer boards to date have been in high density circuits that would otherwise have been designed as multilayers or solderless wrapped panels. When used in place of multilayer printed circuits, wired boards provide greatly reduced delivery time and design and board costs. Design savings of 60 percent are typical while board costs are 25 percent to 50 percent less expensive depending on the quality involved.

When used in place of solderless wrapped panels, wired boards offer the benefits of reduced package size, weight, and cost. Savings of 40 percent to 60 percent in all three areas are typical.

3. *Level Three, Back Plane Wiring*

Backplane systems are constructed of either multilayer PC boards or solderless wrap panels and, in many applications, are a hybrid combination of both techniques. The hybrid backpanel can be described as having a sandwich construction consisting of voltage plane, common ground plane and insulated plates, with solderless wrap terminations providing multilevel signal paths. The multilayer PC motherboard construction employs plated-through hole terminations with common layers of copper as voltage and groundplanes, along with layers of etched copper artwork signal paths.

The standard connector terminals used in backplane terminations, which are known as wrap posts, are provided with either 0.025 or 0.045 in. square tails, depending on the spacing of contracts. Wire wrapped connections are made by wrapping a specified number of turns of solid wire, under tension, around a wrap post having sharp corners (maximum radius 0.003 in). The sharp corners of the wrap post produce high-pressure points, resulting in indentations of the wire and wrap post. These high-pressure points result in a gastight electrical connection with a high degree of mechanical stability. The same wrap post configuration serves as a termination for common bussing of terminals using bus bars and will accept bushings for termination in a voltage or ground plane. See Table 5 for the advantages and disadvantages of wire wrap interconnections.

TABLE 5

Advantages and Disadvantages of Wire-Wrap Interconnections

Advantages	*Disadvantages*
1. Can be automated, increasing wiring accuracy	1. Solid wire only; not standard
2. Features a reliable, gastight connection without plating or other materials	2. Transmission-line techniques unwieldy, system-frequency limited
3. Can use component lead as connection point	3. Close process control needed for reliable product
4. Compatible with rack-panel and drawer-packaging schemes	4. Only effective testing technique is destructive
5. Limited human-factor inputs needed, especially if automatic wire wrap is used.	5. Expensive equipment, tooling and programming for automatic wire wrap

3.4 SYSTEM PARTITIONING

The packaging engineer is faced with the decision of how best to subdivide the system into modules, submodules, and other levels of functional units. The choice is usually complex since many factors can have a significant effect on the decision. The choice can vary from a single circuit unit to a large complex unit of many hundreds of circuits. In general, small functional units permit a reduced number of unit types which in turn enhance spares logistics and manufacturing complexity. Small units are frequently of low enough cost to be considered as throwaway items rather than repairable. The major disadvantage is the increased number of connectors, supporting hardware, and interconnecting wiring required. A large functional module has two advantages: ease of electrical diagnosis and inherent higher reliability with fewer joint interfaces, both of which enhance system maintainability. The final partitioning decision can be made only after a series of trade-off studies considering all the factors listed below:

Manufacturing cost,
Reliability,
Size,
Repair or throwaway,
Maintainability,
Electrical requirements,
Environmental requirements.

The inherent high reliability of microelectronics has made possible the maintenance concept of logistic self-support. It is now practical to provide functional units as replacement units or even built in as redundant elements. A study of the diagnostic requirements will help determine the optimum functional unit size.

The choice between repairing and throwing away units has historically been based only on a flat functional unit cost. With the advent of microelectronics and higher reliability, the military has recognized that reliability is also a determining factor in this decision: if a unit is very reliable, it is frequently more economical to throw it away than to repair it.

3.5 PACKAGING FOR TACTICAL ENVIRONMENTS

Military computers are often called upon to perform under external conditions many orders of magnitude more severe than standard environments. These adverse environments are usually encountered in mobile equipment, such

as airborne, spaceborne, shipboard and ground vehicular. Packaging for missile applications also requires special consideration for surviving dynamic loads. The following discussion presents an example of a packaging technique employed in designing equipment for operation in tactical environments.

Compression packaging is one of the most effective ways to meet severe dynamic environments. The method consists of applying (and maintaining) a predetermined compressive load to the electronic subassemblies within the package to achieve high resonant frequencies. The technique has been used on major space programs.

The compression packaging concept relies on the compressed displacement of a foam spacer to maintain the desired stress. A typical system consists of PC assemblies interconnected via flexible printed wiring through a multi-layer PC motherboard. Each PC has a polyurethane foam spacer bonded to its surface.

The PC assemblies and foam spacer are alternately sandwiched, placed in a housing, and then placed in a loaded fixture where the foam spacers are compressed. Since the PC assemblies are not fixed to the motherboard via rigid connectors, they are free to position themselves. The end panels are then secured to the side-walls of the housing to maintain the desired internal compression after the unit is removed from the fixture. Final compressive force on the package is approximately 600 pounds.

The compression package technique provides protection for electronics under adverse environments, particulary vibration, shock and acoustic noise. The concept provides support for the electronics, provides good vibrational damping and generally, provides advantages equivalent to "potting in place" without the inherent repairability problems.

BIBLIOGRAPHY

1. Danzig, A.C. — *High Density Circuits Using Magnet Wire Achieved With Automated Wiring Techniques*, Insulation/Circuits, July 1974.
2. Douglas, J.H. — *Computers*, Science News, Vol.108, September 1975.
3. Harper, C. (Ed.) — *Handbook of Electronic Packaging*, McGraw Hill, 1969.
4. Holland, C.E. — *Integrated Circuit Reliability and Manufacturing Science*, NELC-TR-1497-2, November 1974.
5. Levinthal, D.J. — *The Computer*, Electronic Packaging and Production, March 1972.
6. Markstein, H.W. — *Interconnection Update*, Electronic Packaging and Production, October 1975.
7. Markstein, H.W. — *Packaging for Detrimental Environments*, Electronic Packaging and Production, August 1975.
8. Schwartz, W.B. — *A Packaging Decision: Multilayer Backplane or Solderless Wrap*, Electronic Packaging and Production, October 1974.

CHAPTER 4

TRENDS IN COMPUTER SYSTEMS TECHNOLOGY

by

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4.1 IMPACT OF LSI-TECHNOLOGY

4.1.1 General Purpose Computers

There can be no doubt that the progress made in semiconductor technology will have a tremendous impact in the fields of data processing and digital control. Until only a few years ago, computers were designed and built starting at the lowest level of transistors and other discrete elements. The resulting circuitry was voluminous, difficult to survey, not very reliable in itself, and very sensitive to environmental conditions. Supply voltage, temperature, and humidity had to be kept to narrow ranges, and protection against shock and vibrations had to be provided. Because of this sensitivity, the hardware was tied to places that met all those requirements. Since computers built up by this method were very expensive, each customer tried to make the best possible use of them. Because of the universal capabilities of computers, each customer had different types of applications. This, in turn, encouraged the producers to make their computers omnipotent; e.g., as powerful as possible for any kind of application. Thus, the hardware became more complex and more cumbersome to program. Thousands of manhours were spent in developing highly sophisticated operating systems and a variety of high-level language compilers. Stages of operating systems were: batch, multi-programming, and time-sharing.

This fight for more efficiency, on both the users' and the producers' part, led to a mutual amplification effect. Truly general-purpose computers emerged, but data processing stayed costly. In spite of a dramatic drop in semiconductor prices and an increasing level of integration data processing, prices did not drop very much for the user because all savings were compensated by increasing hardware complexity and software costs.

4.1.2 Special Purpose Computers

The uniqueness of the general-purpose computer was dispelled in 1966 with the advent of small inexpensive special-purpose computers for business applications. These relatively simple machines, together with a simple and easy-to-handle operating system and a limited set of application programs, became very successful. They were produced by small companies which, in a few years, conquered a considerable slice of the computer business. Even small companies could afford to buy these computers. For the first time, availability, rather than computer efficiency, was of top priority. Compared to its forerunner, this equipment could be operated fewer hours per day without the fear of wasting money. Other special-purpose computers, such as desk calculators, were soon to follow. Engineers and scientists became aware of the savings in time and money possible through use of their own small, easy-to-handle computer in lieu of programming for a big general-purpose computer. The latter involved either walking to and waiting at a terminal or being put into a batch queue several times, plus program bugs and control language problems.

Then came the overwhelming boom of the pocket calculators in 1971, the first token of the LSI-Age, opening a big and entirely new market for digital equipment. Another boom just coming up concerns the digital watch. Some of these are being programmed for digital display and even calculating, years in advance.

4.1.3 Future Trends

Where are we now and what will happen in the near future? First of all, the LSI-technology will affect the whole area of any kind of control. Much of today's special hardware, whether mechanical, hydromechanical, analogous, or digital already, will be redesigned and probably turned over to a microprocessor-controlled digital program.

The reasons for this are obvious. LSI-technology is extremely rugged, small, lightweight, and cheap. There are hardly any environmental restrictions anymore. (See Chapter 2.) Some LSI components allow for a temperature range of -50 to 125 C. Humidity range goes up to 90 percent and supply voltage has only to be kept constant in a range of ± 10 percent. For the same reasons, LSI-technology will eliminate a considerable slice of workload from

conventional general-purpose computers. Small specialized computer systems will withdraw many users and programs from the computers. The economy of time-sharing systems will be questioned and even large multifunctional systems, such as data file handling, may turn out to be better realized with sets of interconnected small computers. Thus, the big computers might very well be left with the big-number crunching problems.

4.1.4 Minis and Micros

Basic elements of today in the design of new application systems are minicomputers, microprocessors, and microcomputers. The attributes,"'mini" or "micro", are not very informative. They just say that those elements are small in size and price compared to older electronics. Be assured that, very soon, we will be confronted with a picoprocessor. Historically, minis are the older ones, originating from the MSI-technology; whereas the first micros are an outcome from LSI-made pocket calculators. These differences do not hold today, because we now have so-called minis which use a microprocessor as their central processing unit.

Generally speaking, a minicomputer has a volume of about 10 liters and an instruction execution time of some microseconds. The word length is mostly 16 bit. A microcomputer, instead, may have a volume of 1 liter or less and an instruction execution time of at least two times longer. However, the latter one is only a figure of today. Microcomputers tend to become more and more powerful; first, because of progress in LSI-technology e.g., increasing number of elements/chip and more sophisticated and complex circuitry; and, secondly, because of progress in high-speed semiconductor technology.

The remainder of this section will be devoted to two areas. The first one will consist of a description of the main components of a computer, processor, and memory and the manner in which they are assembled to build up a computer. The second part will deal with multicomputer systems. It will be shown how micro or minicomputers can be used in cases where a single unit would be unsuitable.

4.2 APPLICATION OF MEMORIES

4.2.1 Main Memory

Modern computers include several kinds of memories, but the most essential one is still the main memory. It is used for storing instruction code and programming input data, intermediate results, and output data. Other memories; such as scratchpad, stack, cache, and associative; are invented and introduced only to increase the throughput or responsiveness of the computers. Read-Only memories are used either for storing static instruction code or replacing hardwiring. The basis on which memories were built from the very beginning of computer technology was called "ferromagnetism". After a short interval, where drums were used for main memory, core memory was introduced. Core technology is still the most important memory technology of today. It has improved very much since the early days. Cores sizes decreased from 2.0 to 0.2 mm and memory read/write cycle time decreased to less than a microsecond. Other techniques based on ferromagnetism, such as plated wire, came up some years ago. Plated-wire memories are more than twice as fast, compared to core memory, because reading is nondestructive. It needs less energy and does not have to be followed by a restore cycle. Writing needs some more energy and, therefore, takes a little longer than reading. The reason that plated wire does not supersede core is that there are still some problems associated with the attainment of magnetic homogeneous plating. Another kind of memory, which is progressing toward competition with core technology even with respect to main memory, is now evolving. This concerns semiconductor memories which have already been discussed.

Depending on the kind of semiconductor technology under consideration, read/write memories have a higher packing density and much higher speed. Present costs are comparable to those of core memory; however, they probably will drop. Semiconductor read-write memories of today are volatile; e.g., they lose all of the information stored in the event of a power failure. However, this does not constitute a real disadvantage for most applications as long as the effects which may result from volatility are eliminated in system design.

First, many cases exist where loss of present information is not disastrous. Here, a means to restart the system would be sufficient.

Secondly, if loss of information is inacceptable; e.g., intermediate results are obtained from long-running programs; recovery points should be implemented by software. "Recovery points" mean that all of the relevant information of a program run is stored on a nonvolatile device such as a disk at certain time intervals. The last recovery point is being used in case of a breakdown. This recovery technique may be necessary because of reasons other than the highly probable failure; e.g., erroneous data, program error, or malfunctioning of devices. Thirdly, in real-time or control systems, downtime is the critical object. Regain of lost information may not contribute very much to the overall downtime compared to the time of repair. Special precautions must be provided for downtime intervals, in any event.

Another type of semiconductor memory under development is nonvolatile. It is called "MNOS" (Metal Nitrid Oxide Semiconductor). This technique allows information storage by the injection of electrical charge to the nitrid

layer. Discharge of the layer takes several hours, but it is hoped to extend this time to several months. Reading is nondestructive and, therefore, fast; e.g., in the range of 100 ns, writing takes a factor of 3 to 5 longer.

Most computer memory systems have a means of detecting data errors. Parity error checking is most generally used. One bit per bytes or per machine word (the parity bit) takes on a certain value in relation to the other which indicates whether or not an error is present. Since parity checking in many cases is inadequate, EDC (Error Detecting and Correcting) can be used. This is well suited for semiconductor storage memories. In this case, a number of bits are added to a data block in memory. The number depends upon the length of the data block. Thus, 1-bit storage errors can be located and corrected, and even some 2- and 3-bit ones can be identified. This well-known error-checking technique will be preferred in semiconductor storage memories because of its small additional costs.

4.2.2 Interconnection Techniques

Requests and data must be transferred between memory and other computer devices (for example, the central processor, the I/O processor). Therefore, a means of fast information transfer is necessary. Because memory can communicate only with one device at a time, requests to memory must be handled according to the priority levels of the various computer devices. Basically, there are two methods of transfer: the "bus system" and "porting".

In the bus system, all devices are attached to the so-called bus, and the bus controller handles the requests to memory. The total transfer rate is limited by the maximum speed of the bus. The bus does not become a bottle-neck, as long as there are only a few memory modules or other high-speed devices (see Figure 1).

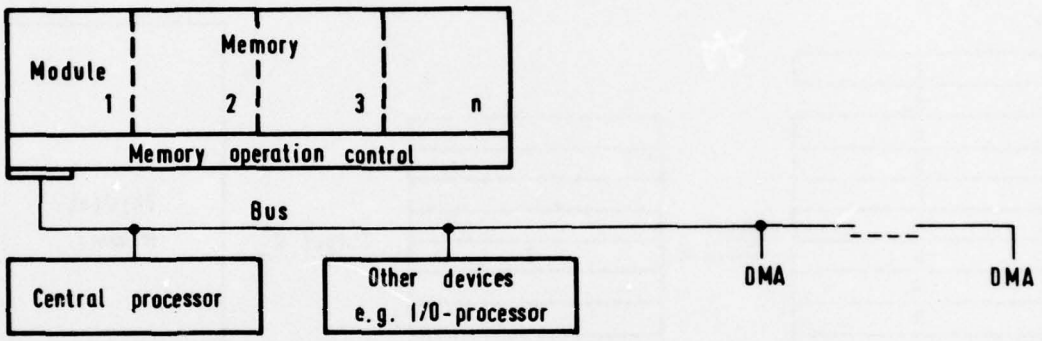

Fig.1 Memory with central memory operation control (Bus system)

In order to increase data processing efficiency, memory can be divided into separate modules each containing its own storage operation control. This provides the possibility of transferring information simultaneously to and from several memory modules. Porting matches with this type of memory system. Each memory module has several parts connected to different devices. In addition, the memory control must take care of sequencing simultaneous accesses (see Figure 2).

4.2.3 Mapping Memory

This type of memory finds great use in computers, with virtual addressing where a virtual page address A is to be correlated to a real memory address X. This is done by using value A as a search key to access a table in the mapping memory. The table element which is correlated to the search key contains the new value X. The mapping memory is often realized by associative memories in connection with normal storage elements. Figure 3 shows an example of this type of memory, also known as "Content Addressable Memory" (CAM).

Here, all memory locations are checked in parallel to ascertain whether or not the value A is contained. The location of value A delivers a coincidence signal which is used to trigger a correlated register and cause the content (the new value X) to be output.

4.2.4 Cache Memory

The price of a storage memory system is very much dependent upon its speed of operation. High-speed storage increases the performance of a computer significantly and is, in general, desirable. A well-equipped computer with a large main memory can, therefore, become rather expensive. This problem can be solved for the case of multi-programming by applying a buffer memory between the main memory and processor. This buffer is called "cache

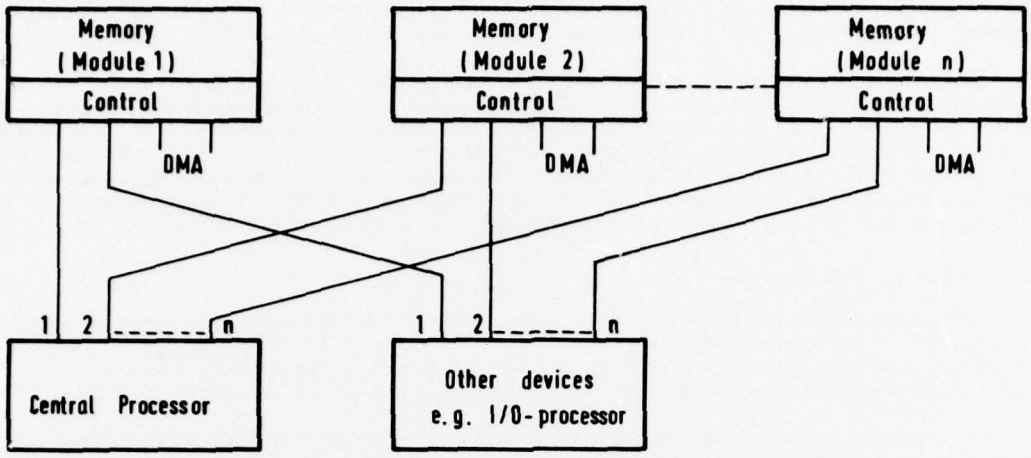

Fig.2 Several memories with separate connections (Porting system)

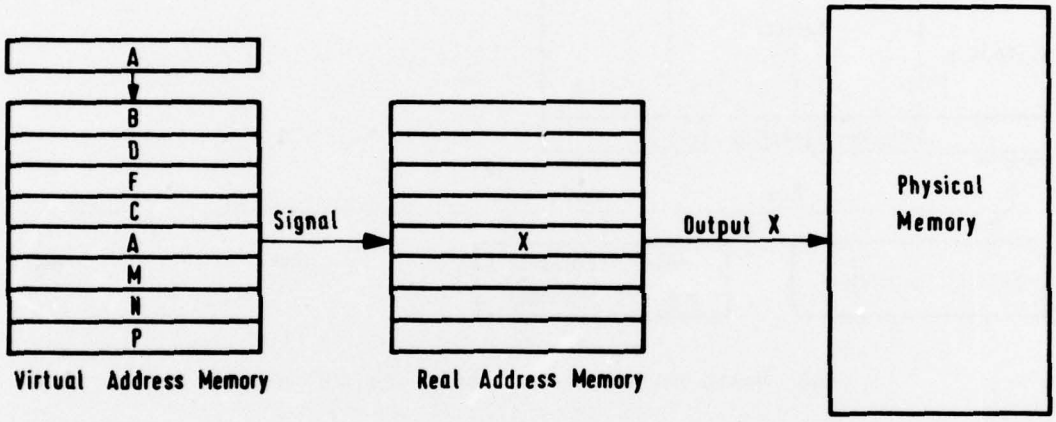

Fig.3 Content addressable memory (CAM)

memory". It is of limited size; e.g., 4 k to 16 k byte; and has high-speed storage capability. The main memory is larger and can be expanded; however, it has a relatively slow operational speed.

Before a program is processed, portions of its instruction code and data are copied to the cache. The processor reads from cache until a point is reached where the required information is unavailable. Processing of the program then will be interrupted, and another portion will be copied which contains the required information. Meanwhile, the processor is switched over to another program a portion of which has been loaded into another section of the cache memory. Restoring of information from cache to main memory is unnecessary if write operation is performed simultaneously into cache and main memory.

The reason for the effectiveness of this method lies in the fact that, generally, data and instructions will be accessed several times during program run. An example are loops. It should be pointed out, however, that this method increases throughput quite impressively (by a factor of 3 to 4) but only if several programs are to be processed simultaneously. It is not very well suited to real-time applications where fast interrupt response is necessary.

4.2.5 Stack Memory

A Stack Memory is used essentially with the interrupt system or subroutine technique. This is a read/write storage area which is used to store all of the relevant information of a running program should an interrupt occur. It is done by using a stack pointer which always indicates the first free location in stack memory. On data input, it is

raised by 1 and, on output, it is lowered by 1. If, for example, 16 data are stored, the stack pointer is raised by 16 and, after output, is lowered by 16. This technique is also called "Last In – First Out" (LIFO).

When a program interrupt occurs, the status of the interrupted program (the working registers and processor status word) is stored in the stack memory. After the interrupting program has been processed, its status is recalled from stack memory and processing of the program continues. The stack memory may be a section of the main memory. Such operations are handled by software. If a very high responsiveness is required; e.g., a minimum time to switch over to another program; a separate stack memory will be preferable. This will be rather small and of high speed. However, because of its limited depth, special care must be taken to avoid overloading.

4.2.6 Microprogram Memory

A microprogram memory is used often today to control the internal functions of a central processor. This memory contains microinstructions which are the switch controls for the gate and storage elements. Each machine instruction calls a *microprogram*; e.g., a sequence of *microinstructions* to be executed. The *microinstruction* has a length of 16 to 128 bits, depending upon the size and speed of the computer. The storage operation control and addressing methods are organized in the same manner as with main memory.

Because of processing speed, a separate microprogram memory with high-speed capabilities is almost always provided. Generally, it is implemented as a read only memory (ROM), with a fixed instruction code. Smaller computers sometimes do apply programmable read only memories (PROM) or random access memories (RAM). When a RAM is used, another storage medium must be provided for long-term storage of the microprograms. After each new initialization, the RAM storage is automatically loaded from this medium. RAM storage is advantageous in that user-oriented instructions or microprogram routines can be established within the system. User-oriented instructions cannot be adapted so easily within ROM storage. However, because design of microinstruction is tedious and error-prone, it often might be better to use only standard instructions, thus avoiding the possibility of severe system malfunctions.

4.3 MICROPROCESSORS AND MINICOMPUTERS

Basically, a microprocessor does not differ from a processor of a conventional computer. It is set up by two main parts. The first part, the arithmetic logic unit (RALU), contains a set of registers and a network to perform the arithmetic or logic functions. The other part, the control unit (CU), controls the functions of the RALU and the information transfer between processor and the outside world, essentially main memory. The major difference between the microprocessor and processors of conventional computers is that a microprocessor is realized on one or a few chips only. This means that it must have a much simpler construction and thus will be much slower. The restrictions are caused by the limited number of gates/chip because of production technique and power dissipation and the number and width of data paths especially pins/chip.

4.3.1 RALU – Architecture

Two major trends in microprocessor architecture can be noticed. The first is directed towards a fixed-word-length ready-to-use processor; the other employs a modular approach with expandible word length, composed by assembling of several chips. Fixed-word-length processors were introduced first. They had a word length of 4 bits and a small instruction set. Standard LSI-processors with a word length of 4, 8, 16 and even 32 bits are now available. These more modern processors exhibit many improvements, among which are:

- Separate address and data bus lines.
- Multiple address modes (e.g. direct, indirect, relative, and indexed).
- Increasingly powerful instructions.
- Vectored interrupts.

These improvements have resulted in a 10-times-faster operation for typical instruction time over first generation micros; i.e., 2 μ sec compared to 20 μ sec.

Modular microprocessors provide slices of 2 or 4 bits per chip which can be assembled to every word length up to 32 bits or even more. This variable word length of course refers only to the width of registers, the arithmetic logic network, and the data paths. The control unit is not affected, meaning that the capability and number of the microinstructions remain unchanged. The processor slices must be interconnected for "carry" and a few other signals. Propagation of the "carry" from the low-order slices to the higher ones (ripple carry) would cause delay proportional to the number of slices. This delay can be cut down if a "carry" look-ahead generator, which can be implemented on an extra chip, is available.

4.3.2 Control Unit

A control unit serves to initialize and synchronize the internal operations of a processor necessary to fetch a

macroinstruction from main memory and to execute it. These internal operations are essentially nothing else but moves of data along different data paths. They are performed by opening and closing gates from and to registers and between data paths; for instance, inside the arithmetic logic network. The gates are controlled by the output bits of the control unit. Control units of microprocessors consist mostly of a microprogram memory and a control network. Sometimes programmable logic arrays (PLA) are used. Factory preprogrammed, they resemble a hard-wired control.

The operation code of a macroinstruction serves as a starting address for the microprogram memory. It denotes the location of the first of a sequence of microinstruction words, which together represent the instruction to be executed. Each microinstruction word alters the microprogram memory address either directly by feedback of some bits to the control network or indirectly by some bits returning from the RALU. The first type of address formation corresponds to an unconditional, the second to a conditional jump.

The operations which have to be performed on execution of a macroinstruction are only partially dependent on each other. Therefore, many of them could be performed in parallel; however, this presumes a sufficient number of independent data paths and an appropriate number of control bits Such will be the case only with processors of large computers which, if controlled by a microprogram, have very long but fewer microinstruction words (horizontal organization). Microprocessors, on the other hand, have a comparatively low complexity. Their microinstruction word length is short and hence their microprogram memories are small but deep (vertical organization). Microprogram memories are mostly ROM's which are factory preprogrammed with a fixed set of instructions. Some microprocessors have either PROM's or even read/write memories which allow the user to extend or to change the instruction set either off- or on-line. This can sometimes be very useful; e.g., for employment in specific control applications, for emulation of another computer's instruction code, or for additional instructions which would lead to a large increase in processing speed.

4.3.3 Microprocessor Operation

A microprocessor is driven by a clock which, in the case of bipolar LSI-technology, may have a cycle time of about 200 ns. This is the time required for execution of one basic microinstruction. More powerful microinstruction may require more time. Viewed from the clock cycle, a microprocessor seems to be extremely powerful. However, this is misleading because, normally, many microinstructions must be executed before the job of one macroinstruction is completed. To explain this, let us assume a simple microprocessor, as shown in Figure 4. It has an instruction register, a program counter, an accumulator, some additional registers, and two buffers for I/O. All of the registers may have a width of 8 bits. They are interconnected by a general bus. Two more data paths are required to gate information from the registers to the ALU. An instruction may have a length of two bytes; the first for denoting the operation code and the second for the operand address. Let us further assume that an instruction has just finished and the next will be an ADD-instruction.

The following sequence will occur:

1. Send content of program counter and read-signal to address bus.
2. Load incoming bit string (operation code) to instruction register.
3. Increment program counter by 1.
4. Send content of program counter and read-signal to address bus.
5. Load incoming bit string (operand address) to register A.
6. Increment program counter by 1.
7. Send content of register A and read-signal to address bus.
8. Load incoming bit string (operand) to register B.
9. Send contents of accumulator, register B, and ADD-signal to ALU; load result to accumulator.
10. Check as to whether or not an overflow has occurred (an overflow would cause a jump to another microinstruction sequence).

The whole sequence will take at least 10 x 200 n sec = 2 μ sec if time for three accesses of main memory is omitted, whereas the internal add – time (step 9) only needs 200 n sec.

Many of these operations can be performed simultaneously. In extreme cases, the sequence could be cut down to two steps, namely:

- Fetch the instruction and operand address.
- Fetch the operand and execute the addition.

However, this is not possible here because it would presume more and broader data paths, broader registers, and more control lines. This sample microprocessor may be oversimplified. However, it shows quite well the limited

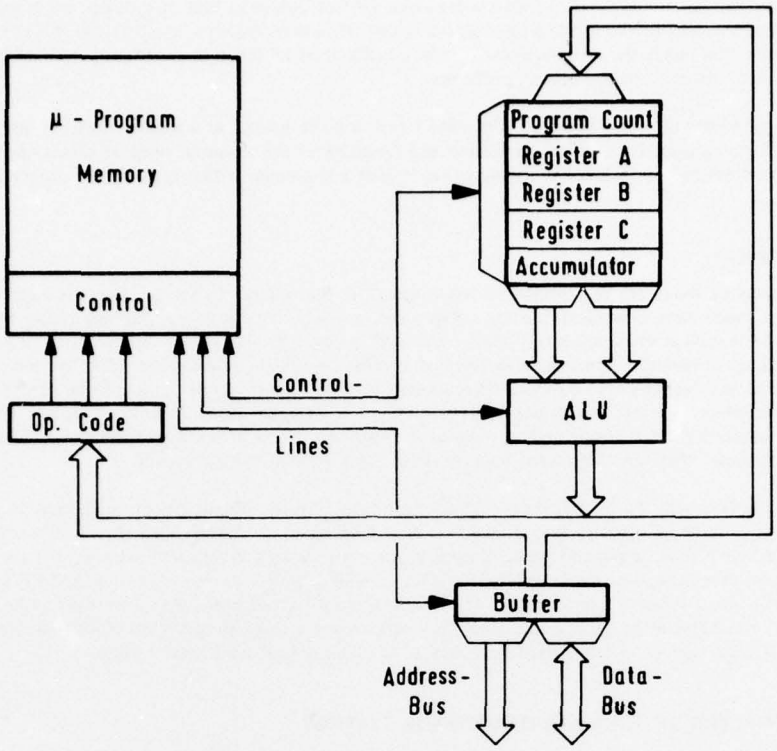

Fig.4 Schematic example of a microprocessor

capabilities of microinstructions which are essentially only moves of data. Furthermore, it might give an idea of the tedious work of microprogramming especially when more powerful instructions than a simple ADD are to be programmed.

4.3.4 Applications Considerations

A digital designer of today must contend with more than the relatively familiar requirements of logic systems. If he decides to make use of programmable components, he will be faced with software problems, and software development may represent by far the major design effort in cost and time. Software development should be performed with tools. Otherwise, coding and especially correctness tests will become extremely inefficient and costly. The minimum tool for coding should be an assembler which could write symbolic instructions code. Far better would be a higher-level language which permits easier reading and cuts down the code length that must be written by a factor of about 10. All of the tiny little coding bugs, which otherwise occur and are extremely troublesome to detect, can thus be avoided. An often-stated objection to this is that higher-level languages lead to machine code which is inefficient and storage-consuming. However, such is not always true. It depends very much on the quality of the translator and, even if the resulting code is not acceptable, the use of the high-level language might be preferable in a first stage to get the system running. Code optimization then can be employed in a second step. A newly designed system will not lend itself very well to software tests because of faulty hardware and lack of adequate means for display of internal states. It might be very useful, therefore, to simulate the system by software on a general purpose computer.

Because the manufacturers are aware of the problems of software implementation, most of them supply customers with aids such as assemblers, languages, monitors, and instruction simulators, as well as hardware. However, it still will be worthwhile for the designer to think of additional software tools. A macro-cross-assembler for translation of a Fortran-like language, for example, could be produced in a high-level language with an effort of about six man-months. Such a macroassembler would, of course, translate much slower than a compiler but that would not constitute a real disadvantage.

Some microprocessors do not even have a fixed instruction code. Instead, they offer to the designer the possibility of defining and implementing a special set of instructions, matched to the application of the microprocessor.

This is called "microprogramming". It presents a far more difficult job than that of ordinary programming. Microprogramming involves the composing of so-called microinstructions which are, essentially, bit strings for control of the information flux inside the microprocessor. Special care must be taken in such an operation because of mutual interference of microinstructions and timing problems.

The microprogram code must be absolutely correct if it is to be loaded to a ROM. However, even when a PROM is used, every programming error requires an erasure and rewriting of the memory, both of which has to be done off line. Thus, if no other means to test the coding exist, at least a test setup with a read/write memory should be available.

4.3.5 Minicomputers

Minicomputers of today are very similar to general-purpose computers. Generally, they are supplied with an operating system, assemblers, compilers, loaders, editors and test aids. Furthermore, they are rather well equipped with peripheral units such as disks, printers, displays, and card or paper tape devices. Programming of minicomputers is, therefore, rather convenient. Some manufactures offer cross-assemblers or cross-compilers and instruction-simulators, written in a higher-level language. This allows the code for the minicomputer to be produced on a large general-purpose machine and thus makes use of its probably much greater capabilities. Cross-techniques are especially valuable, if the minicomputer is to be applied without or with only a few of those peripherals which are necessary for the translation process. The same argument holds if there is insufficient storage capacity.

The word size is usually 16 bit but more recent minis have 32 bits. Floating point arithmetic is often available sometimes optional. Storage capacity ranges up to 32 K or 64 K or even higher. Virtually all of the memory techniques described herein may be implemented. Basically, there are two different architectures: (1) the single bus-architecture where processor, device controllers, and memories have access to one single bus, and (2) the two-bus-architecture which has a separate memory bus. Minicomputers with a two-bus-architecture tend to be more powerful. The unibus concept, on the other hand, leads to a very clear and homogeneous structure both from the hardware and the software side. This lends itself very well to the adaption of additional devices.

4.4 MULTICOMPUTER SYSTEMS/MULTIPROCESSOR SYSTEMS

4.4.1 General-Purpose Systems

The term "multicomputer systems" and "multiprocessor systems" are not very well defined. In this chapter, the term "multiprocessor system" will be used if several processors have direct access to one shared main memory. The term "multicomputer systems" will be used to denote sets of computers which are interconnected; each consisting of a processor, memory, and possibly some peripheral units. The computers may be spread over a large area or be concentrated in one room. They may be tightly coupled by high transmission lines or not. Multiprocessor systems have been in use for many years. The first were computers with autonomous I/O controllers. These controllers relieved the central processor from the task of controlling communication between peripheral devices and main memory. Of course, autonomous I/O controllers do not resemble processors. However, they are capable of executing some operation all by themselves; e.g., transfer of information, simple address calculations, memory access, and some error handling; hence, they are active units. At one time, their very limited instruction set was hardwired. At present, I/O controllers are designed by applying microprocessors.

A next evolutionary stage of multiprocessor systems was the implementation of peripheral processors in large general-purpose computer systems. The peripheral processors prepared the information to be transferred between main memory and peripheral units so that both sides, (central processor or the peripheral units) could directly accept it. Otherwise, this rather primitive bit chewing had to be done by the central processor itself, thus withdrawing a considerable amount of capacity. When the peripheral processors were implemented, they took over additional tasks such as monitor functions. Thereby the central processor was left with true data processing tasks only. This multiprocessor solution turned out to be very economical in spite of the requirement for increased hardware. In addition, the distribution and dedication of different tasks reduced the complexity of the system, thus providing more clarity and better manageability.

Modern multiprocessor systems have not only a large number of peripheral processors but also several central processors which are either identical or designed for special purposes. Another change in system technology is still going on. To a certain extent, it exhibits the move from multiprocessor systems to multicomputer systems. It was marked by the introduction of intelligent terminals. These intelligent terminals are independent units which do their own, increasingly versatile work. They run their own operating system. Communication with the remote central system occurs when more processing power is needed or data is to be exchanged.

4.4.2 Special Purpose Systems

All that has been mentioned so far refers to general-purpose systems. In addition to those, many small multicomputer systems have been designed for special-purpose applications, especially in the area of control. These multicomputer systems consist generally of two or three computers that are interconnected. They are mostly dedicated

systems; i.e., each of the computers performs its own set of tasks. An example of these would be a real-time system to control a phased-array antenna (see references): Here, a first computer is used to switch the antenna beam, adjust the signal processing circuitry, and execute global commands such as searching of a large area or determining the position of a specific object. The first computer receives compound orders from a central computer and returns the results. The central computer performs the overall control and the tracking business. A third computer handles and controls the communication between system and human operator. This system of three medium-size computers is by far cheaper than a single computer which would have to be extremely powerful. Furthermore, matching of the large number of real-time conditions in a single system would present extreme difficulties. Another example is a medical information system built with 10 minicomputers and 60 terminals (see references). The designers believe the cost of this to be a fraction of that of a large computer installation which would handle the same functions.

The minicomputers are all of the same type. They are located in one room and interconnected by a high-speed interconnection bus. The operating system is split up into pieces and distributed over the network. The network, therefore, functions as a parallel processing machine rather than as a ring of independent minis. The whole system remains operable with only 5 of the 10 computers.

4.4.3 Military Suitability of Multicomputer Systems

Multicomputer systems, built on the basis of miniprocessors, seem to be especially suited to military applications. First, there are the components which are:

- highly integrated and therefore small in volume and weight,
- of low sensitivity against rough environmental conditions such as shock, temperature, and humidity.

Therefore, data processing systems which encompass these components can be implemented wherever data processing power is needed; e.g., at a weapon or a device which is to be controlled or at a sensor for data processing and reduction. Because of their inherent power, low cost, and ease of application, microcomputers will replace many hardwired systems as well as specially designed computing systems. In cases where one microcomputer would not meet the needs, several could be interconnected. In this way, more processing power could be provided with higher reliability or lower vulnerability. A multicomputer system with identical components would be easier to maintain and to repair. Its most important effect could be standardization.

The applicability of multicomputer systems is limitless. Their usefulness reaches from mobile units such as airplanes, tanks, and ships to administrative, logistic, and command-and-control areas. The following chapters will provide some examples of these applications.

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REFERENCES

Memories

Davis, S. — *Selection and Application of Semiconductor Memories*, Computer Design, January 1974.

Altmann, L. — *Semiconductor Random-Access Memories*, Electronics, June 1974.

Koehler, H.F. — *Advances in Memory Technology*, Computer Design, June 1974

Torrero, E.A. — *Focus on Semiconductor Memories*, Electronic Design, April 1975.

Reese Brown, J. — *Magnetic Core Memories*, Modern Data, August 1975.

Browers, D.M. — *The Charge-Coupled Device*, Modern Data, August 1975.

Microprocessors

Smith, H. — *Impact of Microcomputers on the Designer*, Proceedings of the 1973 WESCON Professional Program, Session 11.

Hobbs, L.C.
McLaughlin, R.A. — *Minicomputer Survey*, Datamation, July 1974.

Theis, D.J. — *Microprocessor and Microcomputer Survey*, Datamation, December 1974.

Torrero, E.A. — *Focus on Microprocessors*, Electronic Design, September 1974.

Horton, R.L.
Englade, J.
McGee, G. — I^2L *takes Bipolar Integration a Significant Step Forward*. Electronics, February 1975.

Multicomputer Systems

Heart, F.E.
Ornstein, S.M.
Crowther, W.R.
Barker, W.B. — *A New Minicomputer/Multiprocessor for the ARPA-Network*, Proceedings of the National Computer Conference, 1973.

Händler, W. — *The Concept of Macro-Pipeline with High Availability*, Elektronische Rechenanlagen 15, 1973.

Ashenhurst, R.L.
Vonderohe, R.H. — *A Hierarchical Network*, Datamation, February 1975.

Farber, D.J. — *A Ring Network*, Datamation, February 1975.

Wulf, W.
Levin, R. — *A Local Network*, Datamation, February 1975.

van Keuk, G. — *Simulationssystem für elektronisch gesteuertes Radar*, Angewandte Informatik 2, 1975.

Air Force wants Standard Microcomputers for its aircraft Electronics, April 1975.

Carren, D.M. — *Multiple Minis for Information Management*, Datamation, September 1975.

Searle, B.C.
Freberg, D.E. — *Microprocessor Applications in Multiple Processor Systems*, Computer, October 1975.

CHAPTER 5

COMPUTER INTERFACING

by

N.W.Bennée

5.1 INTRODUCTION

5.1.1 Requirement for Interfacing

As the cost of computer hardware continues to plummet and the horizons of computer applicability broaden, the requirement emerges over and over again, for the means to readily interface to and between computers. Modern high performance digital computers offer many undreamed-of possibilities through their sheer processing power and low cost/task. A CPU does not work in isolation, however, and the performance actually realized from a computer system depends critically on the effectiveness and efficiency of the coupling between its component subsystems. Within the devices of a single manufacturer, it would be expected that this coupling had been considered at the design stage. More and more at the present time, however, complex computer systems are configured with components from many different vendors. Quite often this is done for technical reasons, but the invariant outcome is that devices of different origin have to be efficiently and effectively interfaced. Section 5.2 to 5.6 will discuss some of the common types of interfacing problems that can be encountered.

5.1.2 Objectives to be Satisfied and the Problems

Throughout this discussion, the dual concepts of overhead and performance will be used. Overhead is the cost in time or loss of capacity for performing a task through an interface, and performance is the capability actually realized from a device in comparison to its total capability. The objectives of interfacing are then seen as the minimization of overheads and maximization of performance on both sides of the interface. (Cost in cash terms might well play a role in modifying these objectives.)

This task cannot be solved in one universal way, as the ratio of the data widths and speeds representative of processors and external devices may lie anywhere in the range from 1 to 10^8, or even higher. Thus, matching data rates is one of the immediate obvious problems. The signals and signal sequences necessary to control an external device will also vary both in functional definition and electrical specification and this constitutes the second problem to be addressed in this chapter.

5.1.3 Brief Review of Techniques now Possible through the Application of Advanced Technology

This section, as the title suggests, is only intended as the briefest of introductions to the substance of the following sections. Without a doubt, the introduction of integrated digital devices relying for their function on well-defined physical properties of the solid state, has had an enormous impact on the connectivity readily achieved between circuits from different manufacturing sources. The family to which a digital circuit belongs, i.e., DTL, TTL, ECL, (see Chapter 2) etc., means that apart from slight proprietary production differences, the equivalent products from different manufacturers exhibit closely similar properties. Prior to the advent of integrated circuits, a designer was free to design logic in a semi-infinite number of different ways using discrete components. The result was that signal level conventions and circuit drive capabilities were determined by every different circuit designer. The limitation of choice brought about by integrating common functions into standard packages manufactured within a few related families of solid state devices has meant that virtually any component can be connected to any other. 'Limitation of choice' is not as severe a restriction as it sounds, as the industry has produced tailored devices which provide the specific characteristics pinpointed by the discrete designer; for example, high noise immunity, high level logic and radiation hardened devices. Thus, in today's interface jungle, the voltages and drive currents visible on both sides of a hardware interface are likely to fall into, at most, two different families. The ease with which interfacing can be achieved is evidenced by the boom in plug-compatible peripheral suppliers seen in the market place during the last few years.

Of major importance to the military designer is the decrease in power and weight requirements of equipment utilizing this modern technology. Functions previously requiring large fixed installations can now be readily contained in mobile vehicles and complex functions not feasible with yesterday's technology can now be realized.

5.2 COMPUTER/COMPUTER INTERFACING

While this particular problem is extremely interesting and has been solved in many production computer systems, for practical reasons of space this discussion is restricted to the problem of interfacing two processors of different origins. The reader is referred to Chapter 4 where a discussion of multicomputer and multiprocessor systems is presented.

For this type of interfacing to be considered, the requirements for data width and speed of transfer of data must be of overriding importance to the system designer. At the processor level, it is assumed that some means has been provided for communication with the outside world.

5.2.1 Direct Interfacing

Typically, interfacing would take place between the bus structure or equivalent on one machine, and the bus on the other. A bus structure is used here in the context of a collection of signal lines which conduct signals representing data, address or control information, and which are accessible from outside the processor by *design*. (See also Chapters 4 and 7.) Some processors are equipped with several access ports which in effect are independent busses. Interfacing that requires special modifications to processors at the component level is unlikely to be suitable for the type of requirement likely to arise within NATO.

In terms of the efficiency and effectiveness of such an interface, the most serious problem that is likely to arise in a processor with high bus utilization is a decrease in processor performance due to over-commitment of the bus. Signal levels and control sequences in general present few difficulties. The prime applications for the processor/processor link, would be control of one processor, i.e., start, stop, branch to address by another, and when high confidence in the system is required and realized through redundancy or self checking. Interfacing for the purpose of data transfer alone would utilize one of the techniques described in later sections.

5.2.2 Via Common Memory

There are many successful commercial examples of the use of this technique within a single machine. For inter-machine application it is essential that the memory subsystem has (see Chapter 4) several access ports. These are sometimes referred to as direct memory access (DMA) ports. The ports operate autonomously and asynchronously, and allow writes and reads to be made to or from memory from each port. Thus, by simply observing the interface convention of the DMA port, interfacing has been achieved. If the memory subsystem is capable of supporting the total data rate generated by all its access ports, and if each port can operate as fast as the individual processors demand, then there will be no overhead other than that produced by address conflicts, and both processors will operate at full speed. A mismatch of data rates in an asynchronous interface carries no overhead cost in general, only a performance degradation in the faster component. Buffering of data transfers can leave the faster component free to do other work in between loading or emptying the buffer, with a consequent diminution of performance degradation. An example of a requirement for such an interface would be between a high speed number crunching type processor which was performing data reduction, and analysis on data supplied by a real time processor acquiring data from a radar subsystem (see Chapter 7).

5.2.3 Via I/O Channels

The interface between two I/O channels of different processors is perhaps, the simplest to implement. The interface itself can be handled simply as another peripheral with a well defined set of characteristics. The software support of such an interface requires only that peripheral handler programs be written for it in each machine and each machine can be in complete control of its side of the interface. The hardware interface, apart from presenting a standard peripheral interface to both processors, has to arbitrate over who has control and in which direction the data will flow. As the data widths of the different I/O channels are not necessarily the same, the interface may have to perform some reformatting function in order that transfer efficiency can be maintained.

The overheads experienced with such an interface are primarily the same as those experienced when supporting any other peripheral of similar data handling capacity, i.e. if transfers can be direct to memory, the overhead will be lower than if the processor is interrupted on receipt of every single character from the peripheral.

The practical implementation of such an interface presents no real difficulties, as most certainly circuits, or modules of circuits, will already exist to interface with the I/O channels. The problem reduces then to the design of the logic to join the two interfaces[1].

5.2.4 Via Shared Devices

Probably the best example of an application in this area is when several processors require access to a single data base contained on rotating mass storage, i.e. disks, drums. An important aspect of this type of situation is that only a small part, or even none of the data transferred to the shared device on a particular transfer, may be of

interest to the other processors. Therefore, at first glance, it would not be a very good idea to employ a form of interface which would entail interrupting one processor while transferring data that it had no interest in. The shared device or the device controller will have to have multiple access ports, similar to the example of the memory subsystem. (5.2.2).

Again, these port interfaces will have a well-defined functional specification and each computer can treat the shared device as its own, provided that the overall system design has taken proper notice of the requirements for interlocks (software and/or hardware). The relative overheads and performance achieved through the use of this technique is, as in Section 5.2.3, dependent totally on the overheads in servicing the peripheral by the different processors. These factors are discussed in later sections.

5.2.5 Via Communication Subsystems

From the hardware implementation standpoint, this is the simplest form of interfacing as long as both processors support one and the same communications protocol. It is also the least capable in terms of data rate, as the commonly used standards only allow data rates to ~ 50,000 bits/sec. The overheads involved can be quite considerable, as the data may have to be parcelled into blocks and have appended error detecting and/or correcting information. If this task is performed by the main processor, it can be a considerable overhead. A dedicated communications processor can be used for this function (see Section 5.4) and also to handle the transmission protocols between the machines (see Chapter 6). The necessity for this type of interface is usually brought about by the need to have the processors physically separated by more than a few hundred meters. When forced to use this means of interfacing, great care usually has to be taken to ensure that the information content of the transmitted data is maximized.

5.3 COMPUTER/HIGH SPEED PERIPHERAL INTERFACING

In general, the performance of a computer system is determined largely by the performance of its most heavily used components. In many applications these will include expensive mass storage devices such as drums and disks. The freedom to choose the most cost effective configuration built from components of different sources presupposes the ability to readily interface between these components. In addition to the general observations made in previous sections, we will examine in this section how advanced solid state technology has helped to solve the interface problem of achieving performance by minimizing overhead cost.

5.3.1 The Role of the Device Controller

An examination of the control requirements of a typical movable head disk drive reveals that there are several. For example, a simple disk device will need to be told to move its head forward or back one track, to indicate when it has a particular sector of the disk surface under the head, and to read or write the information. Further, it will be expected to perform some kind of confidence check on head position, angular position, error detection on written data, and supply general device status information, i.e., unit ready/busy, disk up to speed, temperature OK, etc. If such a device is directly connected to a data channel of a processor, it can be expected that performing I/O is going to cost a lot of processor time just looking after this device. Indeed, this is still the case in many relatively recent computers in regular use today.

The trade-off, or design criteria used to be – "keep the hardware cheap and simple and to do the clever bits by software". This attitude *was* indeed the only realistic way of making such devices marketable. Integrated logic at even the lowest level of integration (SSI), has enabled the responsibility for the microsecond by microsecond control of complex high performance (high data transfer rate and capacity) devices to be removed from the processor and incorporated in a device controller[2]. The controller can also handle all the communication with the device or devices. (Multiple identical units can be handled almost as simply by using only one controller-to-processor data channel connection.) Given that the data channel is sophisticated enough to perform asynchronous transfers to memory, the processor overhead will be reduced to sending a start address, data length and read or write request to the controller, and then after the I/O has finished, to acknowledge the interrupt and ask the controller if everything went OK.

The controller may have to issue several low level commands to the device to position heads etc., to detect a positioning error, to reset the device and to step through the sequence a hard wired number of times, before an actual data transfer occurs. The software in the processor then has very few decisions to make except for whether to retry an I/O operation that has been detected as failed by the controller. The problem of interfacing to a controller has already been dealt with and is probably very much simpler than interfacing directly to the device itself, and, more important, involves far fewer overheads.

5.3.2 Application of Processors Integral with Controllers

Devices such as disk and tape drives still carry overheads in time, due to the physical design of the systems. It takes a finite amount of time for tapes to rewind and disks to rotate and there are, thus, overheads involved

during these basic operations. Multiple devices on a single data channel with the possibility of overlapping operations on different devices enables the data channel(s) and hence the processor(s), to be utilized at a higher level. While having multiple devices on a single controller is a rather straight-forward problem, parallel overlapping of operations requires complex logic. The viability of building dedicated tailored processors within device controllers came about with medium scale integration (MSI), a level of packing that still enables the function of single chips to be easily perceived and applied in a flexible way. These processors are typically equipped only with a function repertoire appropriate to the tasks they have to perform, but in consequence, they are simple and cheap to make, relying as they do on the controlling program (variously called controlware, firmware, control software, etc.) for their flexibility.

With the blossoming of LSI technology, in particular, semi-conductor memories and processors on a chip, the decision to build "intelligence" (or a better wording is "flexible control decisions") into a device controller is an easy one to access. It has been shown in the market place that peripheral devices exhibiting "intelligence" are readily adaptable to a wide range of different machines. After all, the intelligence is not confined to the device side of the controller; it can also be used to assist in the dialogue with the data channel.

At the present time, the so-called microprocessors on a chip are less powerful than the modern minicomputers against which intelligent controllers for high performance peripherals should probably be compared. However, the success of the microcomputers in the couple of years since their debut is very strong evidence to believe that they will replace "discrete integrated" logic in the applications we have just been discussing. The development, in particular, of microprocessors configured by separate external control micro programs, means that functional characteristics required for a specific application (for a particular controller)[2] can be realized by coding (burning, masking) one or two chips. Perhaps of equal importance is the demonstrated effectiveness of placing a little bit of intelligence at even the lowest level in the processor hierarchy, at the peripheral itself, thus relieving the overworked control processor of some of the more elementary, but time-consuming, control and monitor functions. This procedure immediately releases spare capacity in the device controller for handling additional devices which further improves the overlapping of overhead operations and enhances component utilization. "Big fleas have little fleas", etc.

5.3.3 Flexibility and Cost

These discussions have developed from considerations of interfacing in a general context. A look at the current computer system architecture of most of the leading international computer manufacturers reveals just the same hierarchy of processors that has been developed here. In fact, some machines employing processor hierarchies have been in operation for over 10 years[3]. Originally, the giant computers had to just out-compute every other machine and the cost of such a machine was expected to be high. The wider application horizon seen for computers today requires that they have to be not only powerful (capable), but also flexible and cost effective. Thus, for a given range of computer it is a marketing necessity for it to be capable of configuration for a large variety of different applications.

The practicality of these concepts have been proved by the application of advanced semi-conductor technology.

5.4 COMPUTER/LOW SPEED PERIPHERAL INTERFACING

It has been shown in the preceding sections that the I/O channel is the primary means by which data is communicated between the processor and the outside world. In today's computers, these channels have to be able to handle the fastest peripheral devices, which may require data rates measured in many Mega bytes/sec. To avoid duplication of functions, these same high performance channels may also be the only means of interfacing to slow speed devices as well. Thus, if one teletype-like device was interfaced to such a data channel, the channel's utilization would effectively be zero. Bus-oriented systems do not have this disadvantage, but analogously the bus interface is most likely still capable of considerably higher performance than that necessary to support a teletype. This mismatch leads naturally to the concept of multiplexing.

5.4.1 Multiplexing

Within the context of this document, a multiplexer is defined as a device which collects together many low speed streams of data and produces a total data rate more appropriate to the performance of the high speed data channel to which it is connected. An important element of a multiplexer is the buffer memory, where slow data is assembled into blocks for each of the devices before being transmitted to the computer at high speed. These functions usually work in reverse as well. Many high speed peripheral controllers also perform buffering of data to and from the computer to one or more individual peripheral units in a similar way, but in addition, have to perform control functions which may be quite complex.

Matching of data rates by buffering is not the only technique a multiplexer might use to achieve its ends. Dependent on the system architecture, individual bytes from or to a slow device may have their source address or destination appended to them when travelling along the data channel. In consequence, consecutive bytes or words

or small blocks of data, may be from quite different sources and it is left to the software in the processor to sort it out. Simple-minded multiplexers which are nevertheless quite complex (and expensive) devices when implemented in yesterday's technology, are more likely to be emulated by the intelligent controllers of the previous section in all but the simplest applications. Local support of remote terminals utilizing bit serial data communication is such an example, where the functions to be performed are very simple, and advanced technology has packaged a lot of the logic required into a few LSI chips. Such multiplexers generally have a fixed number of ports onto which terminals or modems are connected, and only require access to the processor's memory, or occasional servicing by the processor to transfer an accumulated block of data. The principal reason for using a multiplexer for this application is that it is a cheap solution when all devices supported are very similar. If a wider variety of devices and communication protocols are to be supported, a little "intelligence" can go a long way towards avoiding headaches and complex circuitry. This "intelligence" usually takes the form of a communications processor.

5.4.2 *Communications Processors*

A communications processor is a computer and, as such, has benefitted from the advances in solid state technology. Its primary role in this section is one of data collection and concentration. In Chapter 6 of this report its application to computer networks will be discussed. It will be seen that in some aspects the communication processor plays a more significant role than the host to which it is connected.

As a computer, the communications processor has a requirement to interface to the outside world; on the one side, to the I/O channel of the host machine(s), and on the other, to the relatively slow data rates of a variety of communication lines. Thus, although a communications processor may possess normal peripherals of its own, its primary function is to service many devices of the same or very similar type. Not only that, but the function repertoire it requires to perform its task is small and very specialized which, in principle, should enable it to be built simply and cheaply. The processor's interface to the communications lines will typically be via a hierarchy of interfaces comprised of several levels. At each level tasks common to the level immediately below it will be performed for several members of that lower level. For example, several communication lines operating at 2400 baud might be serviced by a single 2400 baud clock, while others requiring the encoding and decoding of cyclic redundancy characters might share a common module for the purpose. The image of today's communications processor is one of functional modularity implemented with no little assistance from the arsenal of MSI and LSI technology.

5.5 COMPUTER/ANALOG DEVICE INTERFACING

So far the discussion has limited itself to the movement of information between digital computer-like devices. The information content has always been encoded into a digital representation. The real world, however, has many attributes which do not manifest themselves naturally in a digital form. The sensing or measurement of these physical attributes is very important in many applications utilizing computers and a discussion on how modern technology enables the computer to "perceive" the real world is relevant.

5.5.1 Analog Transducer

Above the quantum level, all classical physical phenomena are continuous in nature. Sensing the measurement of the value of a physical phenomena, such as temperature, which is continuous in value, typically rely on other properties which are themselves continuous. For example, the continuous change in temperature of an enclosure might be measured by allowing a cylinder of gas to be heated within the enclosure. This causes a continuous change in its pressure, which could be detected by the continuous linear displacement of a piston in a tube connected to the cylinder working against the tension in a spring, which could also be sensed. None of these transformations between different physical measureables assists in letting the computer know the temperature. The problem is solved in general in two ways: the direct encoding of a mechanical displacement into digital form and conversion of the physical variable into an electrical analog followed by digital conversion. The former is generally achieved using mechanical contacts sweeping over a segmented conducting plane in the simplest cases or with the use of an optical encoder. The optical encoder can have a very high precision if use is made of such phenomena as Moiré fringes. In essence, a plate which is engraved with alternate clear and opaque stripes is directly coupled to the mechanical movement. The movement of these stripes then alternately makes and breaks a light beam (usually an IR diode source and detector) providing the required digital pulse train at the output. Provision has to be made to obtain the correct sense of the movement and it is usually achieved by employing two displaced sensors. In a rotating environment, magnetic tachometers are also used. Here a magnetic discontinuity (a slot) is made on the perimeter of a small wheel or shaft and its passing is detected by a magnetic pick-up head which then provides an electric pulse.

In the case of electrical transducers, the physical variable which is being measured produces analog changes in an electrical property such as resistance, dielectric constant, charge mobility, etc., which is then directly converted to a proportional electrical voltage or frequency. Voltages may be converted to a digital value by means of an analog-to-digital converter and frequencies may be simply counted during a fixed time period.

5.5.2 A/D and D/A Converter Advances

Analog-to-digital (A/D) and digital-to-analog (D/A) converters are the means of translating information originating as a voltage or current level into a series of binary values. Although single chip examples of these devices do exist, they are normally fabricated using hybrid technologies. The principal parameters which serve to quantify an A/D converter are: its precision measured by the number of bits it uses to encode the analog value and the number of times per second it can perform the conversion process or its sampling rate.

In some applications its ability to handle rapidly changing analog values is also important. The advances in this area are primarily due to a steady increase in performance (stability and speed) of classical components and does not rely on any breakthrough in technology or new philosophy. The greatest application in this area has been the replacement of heavy, slow electromechanical analog sensors and activators by small size low power solid state equivalents. Fire control systems for shipborne guns are immediate examples of beneficial application.

5.6 COMPUTER/HUMAN BEING INTERFACING

5.6.1 The Human Being

Man is the biggest user of his invention, the computer, yet this interface is probably the most complex. Human psychology and physiology are in no way compatible directly with the interfaces associated with computers, yet man's perception and decision-making can be indispensable components in a complex computerized system. Man makes a decision about a situation based on two factors: knowledge or experience of the situation, and current information perceived from the input of his senses. Man has five "directly accessible" senses: sight, hearing, smell, taste and touch, by which means all information about the world reaches his brain. His means of affecting the world are restricted to the control he can exercize over his muscles.

The apparently simple situation is complicated by the idiosyncrasies of the human mind exemplified in human psychology. The simple act of pressing a button to signal some event or request to a machine is not as simple as it might appear. Man's motor (muscular) control is highly dependent on feedback, so the button has to "feel right" mechanically and even texturally. It may even have to "sound right" and in intensive situations where human fatigue is a potential problem, it has to "look right" in form and colour. Thus, the provision of even a simple binary signal to a computer originating from a human being can require extensive behavioural studies to determine the best interface.

Taste and smell are not currently used in the human interface, except possibly to sense that the hardware part of the interface has failed and is about to catch fire.

5.6.2 Input Devices

Buttons still remain the oldest and most commonly found means of passing information from a human being to a computer. While the factors discussed in the previous section are fascinating to discuss, this discussion will be limited to the impact of modern semi-conductor technology. Much has gone into the humble push button since it appeared as the old fashioned bell-push.

Two brass strips and a china knob have evolved into engraved, molded coloured plastic buttons, holding a speck of semi-conductor material containing circuits equivalent to many transistors. Brass contacts have been replaced by exotic materials, such as gold plated beryllium/copper alloy and some designs do not even have contacts.

The fabrication of a Hall-effect sensor, together with some interface circuitry on a single chip, has produced a switch that has no visible means of switching. Contact bounce is eliminated because there are no contacts and the mechanical construction is elegantly simple. A small magnet in the head of the button, which is restrained by a small spring (to supply the "right feel"), is brought near the Hall-effect sensor which, at a present value of magnetic flux, causes a trigger circuit to fire and latch until the magnetic flux decreases below another preset value.

Even "classical" contact operated buttons may utilize a chip to overcome contact bounce problems by using a simple latching circuit. It was just not practical to implement such a circuit in every push-button of a system before the advent of integrated technology.

Mechanical/optical push button systems are also used for keyboard applications where code generation is required. Although code generation by diode array or read only memory (ROM), is straightforward, the use of light emitting diodes (LED) and detectors and mechanical shutters to make or break the light path to produce the codes, has minimum electrical components and minimum complexity.

Capacitive arrays of wires for touch-wire input applications have benefitted from the advances in high impedence field effect devices (FET) and pattern input devices, by the use of charge coupled light-sensitive arrays (CCD)[9].

Input by human speech is an area which has benefitted greatly by semi-conductor developments. The complex signal processing that it is now possible to perform on the analog voice (see Chapter 7) signal before it is ever presented to the computer in digital form would not have been possible with any reasonable size piece of equipment 10 years ago. High performance A/D converters, operational amplifiers and ceramic and digital filters are all devices resulting from advanced technology, which make the realization of voice input to computers a method that will become more and more common[10]. Commercial command recognition systems already exist for some industrial applications.

One can speculate that the use of digital voice techniques will become feasible for the domestic telephone services by introducing the necessary conversion equipment into the telephone handset. This will enable the provision of secure lines for commerce and military alike within the existing network. Further, voice recognition circuitry at minimum would enable automatic billing and the possibility of on-line language translation between countries seems feasible.

5.6.3 Output devices

The principal sense used to perceive output from a computer is that of vision[4]. Reading of printed or displayed text will still be the most common method of information input to the human brain for the foreseeable future. This belief is obviously shared by the electronics industry who continue to invest heavily in research into display devices[5] and techniques. Solid state display devices fall into two categories: active and passive. Within the active categories are the LED devices now available in a variety of colours (red, yellow, green). These devices may either be in the form of an individually packaged diode, which can be mechanically assembled into large arrays of diodes each providing a point of illumination, or prefabricated into smaller integrated arrays of diodes on a single chip. For instrumentation purposes (pocket calculators are included under this heading), the seven-segment displays lead the field. Seven diodes, formed as bars on a single chip of gallium arsenide or phosphide, make it possible to display all the digits and a few letters. For applications where full alphanumeric capability is required, the LED matrix is used instead. However, despite the rapid development and domestic application of these devices, for the display of large amounts of text (1000 characters) they are non-competitive with the older techniques using cathode ray tubes (CRT). Further, requirements for large scale displays or display panels are currently only economical using projection techniques based on the CRT although the application of liquid crystal light cells appears promising.

Despite its antiquity, the CRT has benefitted from advanced solid state technology no less than the more exotic display devices. The development of high voltage transistors, and low work function longlife materials for heated cathodes, has helped to make the CRT module an off-the-shelf, low cost and easily interfaced solution to many display applications. The question of whether or not the development of phosphors or ferrite materials for colour display CRT falls strictly under the heading of solid state advances will be ignored as the new dimension introduced into the man/machine interface by the introduction of colour displays is sufficient reason to highlight the problems.

The mechanics of presenting information in multicoloured form are, of course, not difficult, but the effective use of this ability to communicate the maximum amount of relevant information to a human being, relies totally on our understanding, or lack of it, of the behavioural characteristics of the human being who is watching the display. In this respect, it is true to say that technological capability is still leading our ability to apply its fruits.

The passive category of display devices referred to earlier, all relies on some type of polarization phenomena. The application of liquid crystal displays follows the same lines as LED devices, but with greater advantages for applications requiring low power dissipation. The only power flowing into a liquid crystal display is the displacement current which is a function of the capacitance or size of the display and only flows when the displayed information changes. Dissipating no power, liquid crystal displays are not luminescent and have to be illuminated, either frontally in reflecting mode, or from the back in transmission mode.

The day when computers will speak to us as a normal means of interfacing is not far off[10]. The standards of pronunciation and protocol (etiquette) that will emerge are, again, a matter for the behaviourists. How should a computer address a human when it is trying to tell him he has made considerably more coding errors than the computer would have expected? The technological advances necessary have already been made (see Section 5.6.2); the remaining problems are semantic.

5.6.4 Impact of Advanced Technology in this Area

Apart from more of the same, ever more intelligent terminals, more complex functions being performed locally, etc., the audio interface is expected to find a secure place in the interface scenario. The main advances in true application will, however, rely heavily on the soft sciences. The behaviourist will rule the day.

The example of the head-up display is illustrative of the complexity possible within the size, weight and power conscious environment of an aircraft cockpit. Some types of display monitor the movement of the pilot's eyeball and through a computer direct servos to adjust the associated optical system to keep the display in the centre of the pilot's visual field no matter where he looks. Such a technique would probably not have even been conceived without stimulation from advanced solid state technology.

5.7 OFF-THE-SHELF MODULES THAT SIMPLIFY SOME INTERFACING PROBLEMS

5.7.1 Brief Survey

The impact of advanced solid state technology on the practical problems of hardware interfacing becomes apparent even at the least complex level of standard circuits. Input clamping diodes and Schmitt/trigger input circuits at the chip level, have made the connection of receiver circuits to data or control bus a relatively problem free task. Further chips, specially tailored to provide good line driving capability, mean that getting signals from A to B has become a non-problem area. When interfacing to a bus structure there are limits to the loading that the bus components will tolerate. Tri-state output stages, where the output floats with an effective high impedence when the particular chip is not actually being used have gone a long way to simplify the bus load problem. This technique has been implemented even among some of the simplest chips.

As we ascend the ladder of complexity, we find the components that make complex interface and controller designs possible with a low component count. For example, an 8-bit shift register with up/down capability and parallel input/output possibilities, performs virtually all the functions required for a parallel-to-serial interface, such as might be used with a cassette tape drive. Its single 24-pin package, however, replaces upwards of a dozen SSI chips necessary to implement the same functions. Likewise, presettable binary counters, parity generators, magnitude comparitors and other arithmetic function devices make the implementation of a device controller from a functional design a straightforward task.

So far in this brief survey, the emphasis has been on components, although the line between component and functional module is a fine matter of definition. With LSI, however, there can be little doubt that the word 'component' is rather an understatement. In the communications area, there are international standards for bit serial interfaces, CCIT[6] and EIA being dominant. The modems required for modulation and demodulation of digital data to be transmitted over large distances are now standard components. The present examples in LSI usually consist of a set of a few chips which can easily be included inside the equipment to be interfaced. The single chip modem is readily possible with today's technology, but as there are usually many options offered in modem characteristics, it is likely that a chip set will continue to provide better flexibility. Probably the single largest impact on the communications problem has been the introduction of various universal asynchronous receiver transmitters (UART) and their synchronous counterparts. These LSI chips perform all the complex functions and error detection necessary to transmit or receive characters in bit serial mode. The presentation of a character code in parallel form (i.e., straight from a data bus), plus an external clock and the appropriate selection signals, result in the character being transmitted in serial form with the desired number of start and stop bits in the chosen parity and at the clock selected baud rate.

On receipt of a serially encoded character, the same chip will check parity, framing errors and false starts before signalling that it has a character in parallel form at its outputs. The large number of components that this chip replaces, not to mention the saving of design time to re-invent it for each application, must make it one of the most significant products of advanced solid state component technology.

Microprocessor chips are clearly the present state-of-the-art devices in the solid state field, but are probably not yet packaged in a way that enables them to be simply applied to interface problems. Thus, although microprocessor chips are to be found in many commercial products assisting with an interface problem (managing the different communication protocols supported by a single communication interface, for example), the cost effectiveness of choosing a micro approach (with attendant software costs) must be assessed very carefully for each problem as hardwired techniques can still have something to offer.

5.8 SUMMARY AND IDENTIFICATION OF CURRENT PROBLEMS

It has been demonstrated how advances in solid state technology have had their impact on the solution of the various manifestations of the general computer interface problem.

The physical nature of the currently usable semi-conductor materials and the techniques applicable to mass production of electronic devices from them, has resulted in families of devices which exhibit compatible interconnection characteristics. Thus, the physical problems of signal level and loading have quite naturally all but disappeared.

The problem remains of functional compatibility on both sides of an interface. Here the prospects are not so bright. Unless a manufacturer designs a piece of peripheral equipment with the specific aim of appealing to a wide market, the solution to the problems of interfacing to other systems will remain unique for each system.

5.8.1 Improvements Realised and Forecast

The area in which most success has been, and is likely to continue to be, achieved is in that of remote terminals. Here suitable interface standards exist and any new device which does not support at least those communication standards is doomed to commercial failure. The addition of "intelligence" within the terminal has considerably improved the man-machine interface, while at the same time giving to such terminals the flexibility to accommodate diverse

communication protocols. In fact, we are entering the area of "intelligence with everything"; as microprocessors become cheaper and more powerful, many of the complex interface tasks of the past disappear. If a description can be provided of the way an interface should work, then a micro can be programmed to look after it. The biggest single advance forecast for the next five years will be the production of easier and easier to use microprocessors. The present day exhibits still have to be interfaced themselves, with the consequent expenditure of design effort. Prepackaged microcomputers, as opposed to microprocessor modules, whether single-chip or printed-circuit cards offering very simple possibilities for inter-connection to the application, will undoubtedly herald the next boom in applied solid state technology. It should further be remembered that today's mini-computer is tomorrow's computer on a chip.

5.8.2 Standards Required

Bit serial interfaces have enjoyed considerable success, being one of the few areas where standards exist. Even though transmission rates are steadily increasing, the data rates achievable with the current asynchronous techniques are still low compared to parallel techniques. For long distance communication, however, serial transmission is still acceptable and it is only with local interconnection that requirements are likely to dictate the use of the higher data rates achievable with parallel techniques. Little has been done in this area, which is not surprising when the diversity of individual manufacturing architectures is considered. Instrumentation system requirements have produced specialised or local standard systems, such as the CAMAC[7] system used extensively in nuclear instrumentation, but are lacking a standard that comes anywhere near the CCIT and EIA standards of the communications front. Proposals for an 8-bit wide standard parallel interface system, operating at transfer rates up to 1 M byte/sec. are under active consideration by the IEEE[8], but have not yet been adopted by industry.

Until standards can be defined, accepted and adopted interfacing will remain as the production of unique solutions to unique problems.

REFERENCES

1. – *An Interface between a CDC 6000 Series Computer and a Honeywell 16 Bit Computer*. N.Y.University, October 1969.
2. Richards, C.L. *An Easy Way to Design Complex Program Controllers*. Electronics, p.107, February 1973.
3. – *Control Data 6000 Series Computer System Reference Manual*. Pub. No.60100000, 20 June 1971.
4. Biberman, L.M. *The Perception of Displayed Information*. Plemium Press, 1973.
5. – *Data Terminal Technology – Present and Future*, Vol.II, CRC Report No.1276-2, Communications Research Centre, Ottawa, April 1975.
6. – *CCITT Green Book*, Geneva 1973.
7. Castrell, L. *CAMAC – A Modular Instrumentation System for Data Handling*. TID25875, USAEC July 1972.
8. Loughry, D.C. *What Makes a Good Interface*. IEEE Spectrum, p.52, November 1974.
9. Amello, G.F. *Charge Coupled Devices*. Scientific American, p.22, February 1974.
10. – *Man Machine Communication by Voice*. Proc. IEEE, April 1976. Special Issue on.

CHAPTER 6

COMPUTER COMMUNICATIONS – A REVIEW OF TECHNIQUES AND SOME APPLICATIONS

by

Y.Lundh

6.1 INTRODUCTION

Digital computers are electronic machines which make use of electrical pulses in a systematic way to represent information; to transform information; to store, distribute, present – in general to *process* information. For the various operations a computer can perform on information, systematic and – it is safe to say – highly sophisticated methods have been established to specify and control the processing in detail.

While many tasks in modern electronic systems are actually sufficiently complex to be regarded as one of the proliferous faces of computer technology, and while the applications of computer technology – with emphasis on hardware or software aspects – continue to grow, the need arises to identify areas as professional fields with their own specialities, their specialized terminology, and their relationships with other "technological subcultures".

Some information processing applications, under the heading "computer communications", have many things in common, and may be seen as an emerging specialized field. It is neither telecommunication nor computation in the traditional sense. Although it may (or may not) be used to overcome distance, and it may employ computations as such, computer communications typically make use of established carriers of information and of various processors and systems for the actual data handling, and comprise the equipment and methods which endeavour to simplify the logical parts of communication. The ways in which units contact other units, in which units tell other units what to do, in which units organize and identify information to be transferred, are all main topics of computer communication. "Units" may be computers, processes or programs running in a computer, typewriter terminals, telephone sets – any machine or apparatus which may have meaningful communication with other "units". Economy, speed, security, reliability and general applicability are attributes of primary interest.

Several recent developments will now be outlined, which are interesting by themselves, and which also may be seen as pieces and traces in a pattern: Computer communications. It will be indicated through examples how these techniques may be applied. It is justified to think of them as the basis for entirely new forms of communication.

6.2 COMPUTER NETWORKS

A number of computer networks have been established in recent years, and improved networking techniques are being steadily developed[1]. Typically, they have been built for specific applications, such as

- Air line seat reservation. Systems permit sales and check-in agents over virtually unlimited geographical areas to have instant access to the booking situation, and aid in fast, safe, efficient, and economic customer service and reservation transactions. (The requirements for such systems were probably the first to spur development of computer communications.)
- Stock market quotation and transaction.
- Fund transfers (banking).
- Message distribution within large organisations, for example "the military forces of the United States".

There are numerous nets for a variety of purposes. Some of the large computer manufacturers maintain nets, which allow certain forms of load sharing between geographically separated installations of their machines. Many universities and other organizations having several computers find themselves with different, typically growing, more or less well ordered communication facilities between those machines.

A large community of professional people are associated with such communications. One manifestation of that is the large attendance and the professional scope of large conferences, viz. the "International Conference on Computer

Communication" (ICCC), held in Washington DC, USA 1972; in Stockholm, Sweden 1974; and in Toronto, Canada 1976 (Refs 2, 3).

Special interest is focused on three computer nets for their generalized character and their roles as vehicles for systematic development of computer communication methods. They vary widely in size and state of development. The largest and oldest is "ARPANET". Two more modest and recent efforts are known as "Cyclades" and "EIN".

The ARPANET, developed under the sponsorship of the United States' "Advanced Research Projects Agency" (ARPA), permits various types of computers, having widely different purposes, modes of operation and computing powers, to communicate. The net interconnects computer installations at many sites (mainly at research establishments). It extends from Hawaii, through an extensive net in the continental US to Norway and England in Europe. The network and its traffic have grown continuously since the first small test installations in 1969.

"Cyclades" is a network being developed under the sponsorship of "Délégation a l'Informatique", a French government agency. In its first major version it will connect several host computers in Paris, Rennes, Toulouse and Grenoble.

EIN (European Informatics Network), is a joint effort by a group of European nations, governed by a committee known as "Cost 11", part of an international technological collaborative effort under the governments of 19 European nations. The actual development is done by an Anglo-French industrial consortium ("Sesa-Logica"), and the planned initial network will comprise nodes in Italy, France, Switzerland and England.

Although the networks have much in common, the size of activity, the diversity and experience already established in the Arpanet are so much larger that it is beyond comparison. A few illustrative examples may be of general interest. Computers ("hosts") range in size from giants such as Illiac IV, IBM 360/91, to minicomputers such as pdp 11. Many different computers are connected, pdp 10 being the workhorse.

Research tasks span from various forms of speech processing to analytical mathematics, from routing and storage of messages, teleconferencing, facilities for joint report writing and other novel forms of communication through seismic observation of earthquakes and nuclear explosions.

In these research oriented nets, *resource sharing* has been a key objective. Resources mean not only computing power, but also various aspects of programs and programming, special facilities, and forming of "communities" which can more easily communicate in spite of geographical distance and of difficulties of mutually convenient meeting times.

Various more specialized applications and disciplines are growing from these broad research activities.

6.3 DIGITAL TELEPHONY

In this chapter we shall discuss a rather different aspect of communication processing. Speech circuits, telephones, and various logical functions, such as dialing and switching, can be handled by digital methods. In fact, any automatic telephone exchange office can be regarded as an information processor. As such, they are even quite large, although specialized.

Even the speech itself can be digitized, converted into streams of binary digits which can then be handled by computer type circuits and methods developed for computers. Above all, it applies to switching.

The many-sided problems which have to be solved by a switching office can be handled by digital computers. This is being done increasingly, and all major telephone organizations have been deeply involved in one way or another during the last decade. One good example of this type of equipment is AT&T's No.1 ESS (= Electronic Switching System), which was described in great detail in Reference 4. It uses electromechanical components for the actual call circuits, but these are entirely dependent on control by digital computers. The main objective is to facilitate certain new, improved telephone services and to increase flexibility and to lower the cost of installation and maintenance while maintaining the high reliability required in permanent telephone installations.

To do the switching by entirely electronic means i.e., avoid electromechanical, moving parts, has long been a great goal, although there is no single all-electronic system which can be said to be "established beyond doubt". Most promising for all-electronic switching are systems which rely on speech being digitally coded. These require each telephone connection to have or to make use of digital encoding and decoding equipment. The resulting digital pulse stream can then be handled by the switching circuits in much the same way as numbers in a computer. Thus, computer circuit technology and system techniques become applicable to all the specialized requirements of telephone switching. The switching itself can then be made rather efficient. Increasing use of digital transmission systems also enhances the attention which such switching systems receive. The chief difficulty lies in the fact that all telephones need digital modulation. So far this fact has made digital switching methods vulnerable in the economic competition with analog methods.

With the continued rapid progress of circuit technology, viz, large scale circuit integration and other fields where intensive development takes place, it is reasonable to expect that new developments will change that situation. There are specialized fields where additional requirements have already done so, viz military communication systems.

One such system, under development by Laboratoire Central de Télécommunications, near Paris, France[5], for application in the French Army, employs all-electronic switching and pulse code modulated (PCM) speech.

Another similar system, under development at the Norwegian Defence Research Establishment, employs modern computer circuit techniques in a concept called "Node Technique"[6]. In this technique PCM is used also, Figure 3.1.

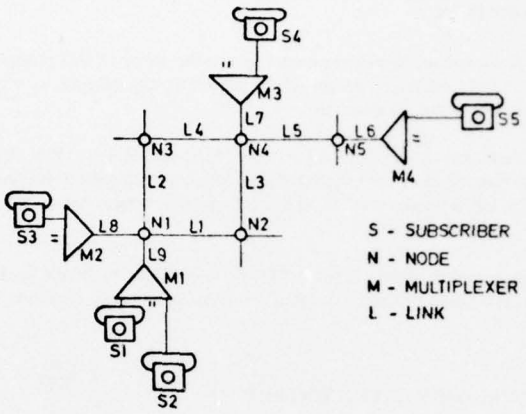


Fig.3.1 An example of an all-digital switched speed system

Each "node" is a computer-controlled switching office of 120 PCM speech channels. It has four "ports", each carrying a time division multiplex (TDM) of 30 duplex channels. Node ports can be connected via suitable transmission links to ports on other nodes or to "multiplexers". Each multiplexer handles up to 30 subscriber telephone sets. The remarkable thing is that each node is now a compact and inexpensive unit (Fig.3.2) although it performs all switching

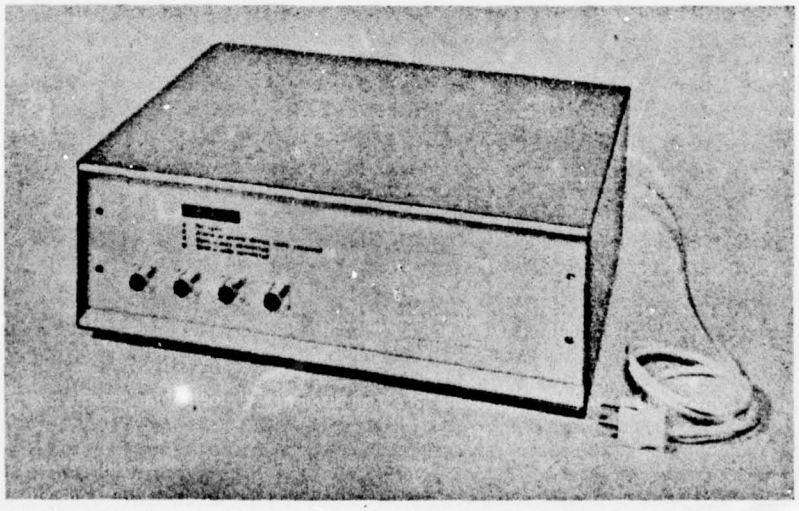


Fig.3.2 Experimental "node", incorporating a computer controlled PCM switch for 120 telephone channels, automatic network routing etc.

and routing functions. It allows new nodes to be plugged in and accepts traffic load in a dynamic situation. Essentially without direction, it performs alternate routing where appropriate, and can be allowed to grow into nets including several tens of nodes.

There are several ways to code speech, in addition to those standardized by CCITT. More compact forms are likely to become feasible with further advances in computer technology. They are of potential interest in specialized applications. Factors which may justify highly compressed speech encoding include extremely expensive transmission channels, special security requirements, computer handling (understanding, storing, generating, etc) of spoken messages. Experimental work on speech processing indicates the feasibility of representing speech with bit rates as low as 2000 per second and even lower, while preserving surprisingly high quality.

6.4 TRANSMISSION AND SWITCHING

A comprehensive review of transmission techniques is beyond the scope of this report. Digital data transmission, as such, is a field under development, and is, of course, interrelated with the need for communication between computers and system parts. Comprehensive literature is available.

Where telephone circuits exist, use is made of such circuits if the performance is acceptable. By "modems" (modulator-demodulator units) it is readily possible to transfer data over standard voice channels at rates up to 1200 bits per second. Higher rates are also being used, up to 9600 bits per second, depending on the type of voice channel and the acceptable error rate.

Still higher data rates require special arrangements. This is generally no technical problem. Typically, such connections employ a larger part of a transmission system carrying a multiplex of many channels, and appropriate modulation techniques.

6.5 ROUTING, NETWORK TOPOLOGY, FLOW CONTROL

In a network having N nodes, Figure 5.1, there are many ways in which the nodes can be interconnected.

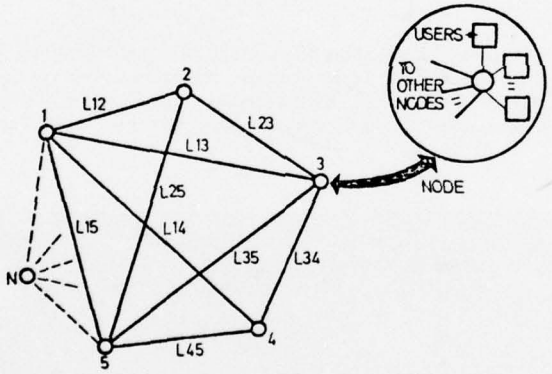


Fig.5.1 A network model, N nodes
To each node users are connected

Nodes in this model are connected directly to each other and to users (i.e., computers, subscribers, terminals). A node is a communication processor (implemented by a "computer"). Its main function is to permit users to communicate.

Figure 5.1 indicates a situation where each node has a direct connection to every other node. At first glance this may seem ideal. That, however, is not necessarily so when considering the problem of achieving economical, reliable communication. Since distance, prices and traffic load are different for each transmission leg, and since it is desirable to avoid one or a few legs failing temporarily, causing traffic to be blocked, the optimum network topology is not necessarily the "fully connected" one.

For example, if the direct route from node A to B is blocked, there may still be a route from A to B through other nodes. As another example, traffic between A and B may be too low to justify a direct line, if the traffic can at all be routed from A to B through the net otherwise.

Studies of network *topology* consider optimum configuration, given the traffic demand and other relevant factors. Optimum networks are almost never fully connected with direct routes between everyone. However, from reliability considerations alone, one can easily see that each node should preferably have more than one link to the rest of the net.

Several modern transmission systems for large numbers of parallel channels are "digital in nature" in the sense that the basic carrier is essentially directly modulated with a very high pulse- or bit rate. One example is the Bell D2 system[8]. The high speed bit stream is time division multiplexed, i.e., a relatively small, repetitive time slot is reserved for each channel. The multiplexing and demultiplexing are done by digital logical circuit (i.e., "computer"-) techniques. The information to be transferred then has to be digitally coded, whether it is voice, television, broadcast quality sound — or digital data. Where such digital transmission systems can be used, they have an economic advantage over analog circuits for the transfer of information which is already digital. All digital transmission systems are, however, far from being generally available everywhere, although they are expanding their territory. A comprehensive digital system for telephone circuits, has been standardized by CCITT[26]. This system employs 64 kb/s pcm for each voice circuit. It is rapidly spreading in many countries.

The transmission rates referred to above represent continuous bit streams. Many systems need only short bursts of transmission, however. Typical situations are those in which computers or computers and remote terminal equipment exchange messages, much like a conversation. A more interesting performance factor than *data rate* then becomes *response time*, i.e., the round trip time for a message of some given maximum length (number of bits) from one point to another and back. Since most data traffic is indeed "bursty", special schemes for utilizing the transmission circuits become interesting, and allow dramatic economic improvements over a permanent, fully occupied line or channel. Such schemes may be employed to achieve lower cost and/or shorter response times. Both in turn open up attractive possibilities for efficient interaction between computers and operators.

"Message switching" or "packet switching" are variations of the utilization of data transmission channels. In a packet switching scheme, there is a communication processor of some kind at each end of the transmission channel, between the user (computer) and the line. It "packs" the information into packets at the transmitting end. Each packet will typically comprise a maximum number of bits, say 1000, from the message to be transferred, together with destination and source address, self check bits etc. The communication processor handles several users, and the total traffic results in a stream of packets. At the receiving end, the communication processor receives the packets, identifies and orders them, and reassembles the message for the destination user. One message may take one or many packets. In a network, there may be many nodes with a communication processor at each node. It must then also have the capability of handling packets in transit according to some routine strategy. "Message switching" implies that messages of arbitrary length are transmitted without being fragmented into packets. The main difference between "message" and "packet" switching is that the limited size of the *packets* allows the storage of entire packets in the communication processors of the net. The use which can be made of high speed storage of *messages* is more restricted.

Packet switching is in use in dedicated computer communication networks. Such networks normally use permanently leased transmission lines between nodes.

Data transmission is available as a standard service from the carrier utility companies in various countries. These services are in continuous growth both in volume and in number of standard services offered. They comprise, primarily, various ways of using voice circuits, but also more specialized systems. As an example, the Telegraph administrations of the Nordic countries have under development an exclusive "data net" (Reference 3, paper T4224). That net will offer rapid switching of data circuits having various transmission speeds from 600 through 9600 bits per second. As another example, the British Post Office has under development a packet switched public data net. Similar programs are in progress in other countries. International standardizing organizations are actively engaged in the tedious processes of standardization etc of these developing communication forms.

Not only are the technical questions important. In the area of data transmission, especially internationally, but even on national circuits, there are many economic, political and legal problems. These, normally referred to as "tariff questions", are among the factors which decide the way in which public transmission facilities will develop, and the speed of development.

Recent advances in electro-optical transmission technology bear considerable promise. Very light and inexpensive equipment is foreseeable for transmission systems for high data rates. They could employ propagation in glass fibres or through the atmosphere at line of sight.

An optimum net will have more than one route from A to B. Which one to choose is a "strategic" question. The routing strategy must be built into the communication processor. Again, what that strategy should be is no simple problem, and will depend upon several factors such as how dynamic, or how stationary the network topology is. It further depends on variations in traffic, reliability factors, and, of course, on economic details. Analysis of this subject in extensive detail is available in the literature[9,10].

As a simplified conclusion, one can assume that any node should have two or more connections "to the rest of the net" for reliability reasons, and that the traffic demands between each pair of nodes in the network, together with economic factors, should determine the network topology in a composite optimization problem.

If we assume a given network topology at a given instant in time, the optimum route between nodes A and B can be defined as the route which gives minimum transmission delay of each packet from A to B. This will depend on the traffic situation in the nodes along the alternative routes, and on the speed of each transmission leg.

Routing need not be optimum, however. Other considerations are also important. Let us look at two different cases. In the "Node Technique" discussed previously, the net is allowed unlimited dynamic flexibility. Nodes can be added or removed freely at any time, and the communication processors will search for a route to the desired user in a situation where each node knows nothing more about the net than what it can observe as being directly connected to it. The search strategy for this situation requires finding "the user" (i.e., subscriber) and "a channel to him". This strategy would be extremely wasteful in a situation, such as the Arpanet, where the subscribers are computers which generate bursts of packets, and which tolerate very low transmission time in their interaction. As another example, in the Arpanet, each node has, in principle, a table stored in it which directs the traffic to each subscriber in the net. This table is different for each node. It is, however, continuously updated. Routing is thus changed according to dynamic factors in the net, such as changing traffic load, change of network topology (e.g., due to temporary break-down), and perhaps even evolutionary changes due to development of routing strategy. Practical considerations such as those illustrated by these two examples, in addition to more or less well defined optimizing criteria, are important in deciding how calls or packets should be routed through a net.

In all cases discussed so far, there is a need for the exchange of packets of information between near or distant nodes in the net. Such traffic requires various forms of queues to be handled. Storage space must be available for packets in transit and for outgoing and incoming packets. Queue lengths and buffer space are important design factors for communication processors. They are, of course, intimately related to strategies and other factors. Again, we shall not attempt to discuss the subject in full detail, but rather refer you to the literature[9,10]. The following facts should, however, be borne in mind: traffic will be stochastic in nature, and any practical buffer size is bound to be exceeded from time to time. The communication processor must be capable of meeting this situation as part of its normal routine. The users should not have to worry about this technicality, but should expect the communication to have a given reliability. The fact that the communication processors may have to establish routines for *flow control*, and that they must be capable of retransmitting, rerouting, etc. to achieve reliability and other performance factors, is one of the design criteria for the communication processor.

Another side of the question of flow control is *where* the buffer space should be. At the two ends of a connection between two users, there may be a choice between having the user itself provide buffer space and/or flow control measures, and leaving it to the communication processor. There is a difference of opinion about where this boundary line should go between functions of the communication net and those of the users. The question is not a trivial one, and involves both technical and non-technical issues. Among these are methods of billing, if the communication net and the users belong to different organizations. Such questions are commonly referred to as "tariff questions".

6.6 PROTOCOL

Communication in the restricted sense of "exchange of information between A and B" requires A and B to have an agreed way of coding the information. Protocol is that agreement. Several details and examples are given in this section. Many readers will find these details unnecessary during the first reading, and may skip to the next section without difficulty.

Depending on what, who, and where A and B are, different protocols are required. In the case of two computers "talking" to each other over some communication network, there may be several different protocols involved. Let us start where we left off in the section on transmission and switching. Information needs to be formatted or packaged into portions of suitable size in order for the terminal equipment at each end to make use of it. Items in these formats are bytes, words, frames, headers, addresses, etc. In the case of packet switching, "packets" of a given maximum size consist of a finite string (for example 1000) of binary digits or "bits" (ones and zeros). Some of these represent the actual information being transmitted, and the rest are required for the transmission itself. The latter includes information such as destination and source, type of information being transmitted, special priority or routing information, packet number (each packet may represent only part of the total message or information flow), checking information (allowing the receiver to verify correct transmission) etc. The method and format in which all this information is laid out as a finite string of bits could be named "line protocol", "packet protocol", or "transmission protocol".

The "payload information" can be looked upon as going through several hierarchical levels or "onion shells" of coding. One way to illustrate this hierarchy follows: Assume a computer program for some computation to require *cosine* to be computed. A typical scientific computer will already have a cosine routine stored in the library that comes with the machine. The programmer can write in his program something like Y = cosine X. This causes the compiler to signal the operating system that "here we need you to take this variable X and have your library program 'cosine', use it and give me the result, which we shall use as Y". Here we have already gone through two levels of protocol, if we desire to define it that way: The programmer used his language or "protocol" to express to the compiler what he wants, the compiler told the operating system, probably in completely different terms (i.e.,

another protocol), what it wants. Now, the operating system will have to make use of that library program. Suppose that the computer did not have "cosine" in its library, but instead, the operating system knew that one was available at a different computer C_B, which it has access to through a communication medium (network). Our computer would then have a communication program or "network control program" (NCP). The operating system would give the NCP an order such as "give this variable X to computer C_B and have it return Y = cosine X". NCP would establish contact to the NCP of computer C_B and give it the order in their (NCP) protocol. The actual transmission of this information would take place in the form of a number of packets being sent back and forth between the NCP's, in a generalized "handshake procedure" which basically ensures that the order is reliably transmitted, understood and verified. This procedure is somewhat complicated because of the requirement that the NCP's must be able to handle many such requests in parallel (actually in sequences which overlap in time), and must be able to keep them separate.

In this hypothetical case we have used the following hierarchy of "protocols":

- programming language,
- compiler to operating system,
- operating system to NCP,
- NCP to network,
- network transmission.

We look upon it as a hierarchy, meaning that each higher protocol makes use of the lower ones. Another aspect of this hierarchy can be seen as follows: on each level, the user acts as if he talks directly to his "opposite number" at "the other place", although in reality he talks to the next lower level "here".

Thus, to any "user" who wants to specify some communication between A and B, a set of commands is available for specifying that communication in the "user to user protocol". In our hypothetical example, the programmer only wrote Y = cosine X. That in reality is a command to the compiler, which in turn gives a command to the operating system, and so on. The programmer acts as if he were talking in a world of mathematics, saying "cosine". The compiler, having identified that as something which a particular program can do, says "get access to program cosine". The operating system, knowing the program to be available at computer C_B tells NCP "get this command to computer C_B, I am waiting for the answer". The NCP calls up the communication processor, saying "get me computer C_B so that I can transmit and receive messages". When NCP has that connection, i.e., it is talking to C_B's NCP, it says "accept this command and give me the answer". In C_B a similar "command chain is activated" – and eventually after computation and return by the same route, the operating system of the first computer can say "here is Y".

This example is hypothetical, and serves only to illustrate the concept of hierarchical protocols. Many concepts are under development in various computer communication projects, and even a survey of these would take up too much space here. Discussions of the subjects are given in the literature[11,12,13,19].

Recently there has been increasing interest in being able to have different computer networks communicate with each other through some interconnection and a mutually accepted "internetwork protocol"[14].

Thus far, most advanced system of protocols seems to exist in the Arpanet, where one main goal has been to allow different types of computers to communicate[15]. The main protocols in this network are:

"Imp-Imp"	– Transmission between network nodes
"Host-Host" and "Initial Connection"	– Between computers (corresponds to "NCP" in the example above)
"Telnet"	– Facilitating the use of operator terminals for several timesharing systems available in the net
"File transfer"	– Transfer of data or programs, stored as "files"

Considerable experience is being accumulated through the use of these and other protocols, and is important in the evolution of generalized methods for computer communications. Considerable changes in protocols are forecast during this evolution.

6.7 TYPES OF TRAFFIC

Many different uses of computer communications are already a fact, and many more will undoubtedly evolve. Let us briefly review some of the ways in which computers can interact. In a hypothetical example in the section on protocols, we described one computer using the services of another as if it were a subroutine in its own program. That indeed is one possibility.

Another form of interaction is the use of a common data base. Some distributed systems make use of common data. There may be several computers each having operator terminals, which allow the centralized data base to be instantly available to all, and to be kept continuously updated. Many different types of uses exist for such systems. Motivation for common data bases may also be purely economical. Very large memories may thus be made available to many users who could not have afforded them separately. The possibility of having remote data bases also allows new freedom in protecting information by means of duplication, "putting away at hardened sites" etc.

Similarly, very large computing capacity may be made economically available to many users through network techniques. Or seen from another aspect: the ultimate size of computing power can be used economically only if many users share it through suitable communication facilities.

Time sharing, in general, is, of course, the basic idea. In recent years many more specialized applications of interactive computations have been pursued[16]. Again, these become especially meaningful if they are interconnected through generalized networks. Among such applications, let us mention a few:

- Computer aided design, for example, of electronic circuits, or of ships or of roads, is a large area of research and development, where many different programs are constantly being developed, improved and used together, interactively and together with manual processes in a constantly evolving process of improved design methods.
- Collaboration in intellectual efforts by people who are separated geographically and have different work habits. For such efforts, there are special communication facilities being developed[17,18]. These facilities are helpful in carrying out discussions, joint report writing etc by several people.
- Special uses of computers under development may in general benefit from collaboration between different research groups if appropriate means exist for practical use of each others programs, data or ideas.

Above all, the interesting thing in common with the various uses and developments associated with computer communications, is a generalized method for interaction. This means that equipment, programs and people, each dedicated to specialized tasks, can easily help each other.

6.8 PACKET SWITCHED, BROADCAST-MODE RADIO COMMUNICATION LINKS

An interesting outgrowth of packet switching techniques is a special method for use of satellite and terrestrial radio systems. Such use has been proposed, and comprehensive studies are being made, although it is not yet known to be in extensive practical use. The basic idea can be understood as follows:

Assume a satellite and many ground stations. The satellite can receive a signal (bit stream) and broadcast it. Any ground station can send signals to the satellite, one at a time. All are able to receive the broadcast from the satellite. It is possible for the ground stations to send only bursts of bits, packets including destination address, etc. Each ground station receiver is thus able to pick out the appropriate packets from the incoming stream. The result is, in effect, a direct link via the satellite between each pair of ground stations.

Several methods can be used for the time allotments, and extensive studies are being made of the practical and economical aspects of the different methods (Reference 13, pp.291-344). Low cost ground stations, e.g., for use on board ships, is one of the possibilities. The latter would rely on a "less efficient" use of the satellite than would be the case with larger ground stations. Extensive work in this area has been done by the University of Hawaii. Their system is named "Aloha"[20,21]. In favourable cases, as much as two orders of magnitude of economic gain seem feasible (Reference 13, pp.329-344), for typical bursty data traffic.

Ground radio communication systems are feasible using similar techniques. Methods referred to as "packet radio" are currently under investigation[22]. Such systems can employ centimeter or millimeter wavelengths, very small portable terminals, and small repeater stations to overcome line-of-sight limitations. They could employ spread spectrum modulation techniques[23] and are promising for operational convenience as well as for conservation of radio frequency usage.

6.9 COMMUNICATION PROCESSORS

"Communication processor" is a term which has been used rather loosely in the previous discussion. Each node in a network has a communication processor. Physically, this unit is typically a minicomputer attached to special hardware for formatting (parallel words to bit stream etc). It comprises interfacing to users and to modem equipment for line transmission. "Users" may be computers ("hosts", "subscriber computers") or terminal equipment such as interactive teletype or similar equipment, remote job entry terminals, or more specialized units. Recent developments in microprocessors will permit many types of communication processors to be very compact and inexpensive in the future. It will therefore be feasible to include such system functions as components in compact equipment.

The processor must provide the user with a standardized way of interfacing with the communication net, and must execute routing and switching functions, including transit traffic between distant nodes. Included in the functions are buffer storage and flow control. Philosophy differs between various experimental networks concerning where the actual boundary lines should go between functions of the communication processor and those of the users. Thus, there is a difference between the proposed European Informatics Network ("Cost 11") and Arpanet. In the former more of the buffer and flow control has to be done by the "Subscriber computer", leaving a simpler task to the "Network Switching Centre" machine (communication processor).

The Arpanet has two types of communication processor in operation. The basic one is the "IMP" (Interface Message Processor). The TIP (Terminal IMP) is an IMP with an extension which allows simple terminals, such as teletypewriters, to be plugged in directly, in addition to and independently of "host computers". This has become a successful general way for accessing a choice of different time shared computers (hosts).

Other communication processors under development under the Arpanet program are the SIMP (satellite IMP, for experiments with packet switched satellite channels) and a multiprocessor version of the IMP which makes it more adaptable to varying load situations and to the reliability requirements of network operation[13].

"IMPs and TIPs" are mentioned here as examples only to illustrate typical functions which can be performed by communication processors in future communication nets.

For specific communication systems to meet specific operational needs, communication processors will be designed into the systems, as component parts. Their detailed implementation can have many variations.

6.10 SECURITY ASPECTS

When more people have access to a system, such as will normally be the case when a system is connected to a net, security problems become more serious and more difficult to solve.

The main things which can go wrong either by malicious intent or by accident are:

- Programs or data stored in a computer may be destroyed,
- Programs or data may be improperly used so as to cause harm,
- Improper use may represent loss of revenue.

Many techniques can be employed to prevent such improper use or destruction. Security in transmission, i.e., ciphering so that understanding the message requires a code key, is one obvious method, but not sufficient in more complex computer networks. In addition, various schemes for controlling access are applicable. These may include more or less elaborate systems of passwords, stringent procedures, access limited to special terminal locations. Security is a field in itself, it is in development, and has many facets. The details of this field cannot be treated satisfactorily within this limited text, but a comprehensive literature exists. Surveys of the problem areas are given in References 24 and 25.

Common to all security schemes are the tenets that protection can never be complete, and that they will be costly. The very highest security protection cannot be combined with network operation. However, very high security protection can indeed be achieved and will quite often not degrade service significantly, if the use is limited to specialized and well defined tasks. Security limitations have not prevented large international computer communication networks from becoming commercial realities for many technical, commercial and scientific purposes.

6.11 USE OF VIDEO CABLES

The "wired city" is approaching reality. More and more cities have extensive cable networks in which practically every home has direct reception from many channels. Typical cable TV systems may have between 10 and 80 channels. This transmission capacity is indeed enormous, and has led to various speculations. Some systems are known to be in experimental operation in limited areas, where subscribers have special equipment added to their standard television receivers. Using special, dedicated TV channels, this equipment can "grab individual frames" in the stream of picture frames being transmitted at 25 or 30 per second. Combined with computer controlled frame transmission, that means effectively that many subscribers can have individual transmission channels for transmission of "static" pictures. Such systems can be made interactive by sending command information from the subscriber via telephone.

Widespread use of such techniques is not known yet. The technical potential is there however, for new forms of telecommunication.

6.12 PREDICTIONS AND IDEAS

Based on the knowledge of technological development as it exists in the laboratories today, and on operational needs, it is possible to describe a few systems which are feasible, and which may become realities in the foreseeable future, say within the next five to ten years.

6.12.1 Tactical Telephone System

A tactical situation is illustrated in Figure 12.1. Automatic telephones are available at command- and other positions where required. All the equipment needed is portable, and can be operated on batteries. The switching office, exchange or "node", for example, is a small portable unit which can accommodate as many as 120 telephones and/or be connected to other nodes to form a distributed switching system. The net is flexible so that it can be expanded or reduced by simply plugging or unplugging, while the parts which are in operation remain unchanged. Alternate routing, where applicable, is automatically handled.

Connections to other telephone systems and mobile radio access systems are straightforward, as are high capacity data transmission circuits and secure voice circuits.

Such a system is envisaged as having high flexibility and other desirable operational facilities, as well as high reliability under war-time hazardous situations, and still be low priced. It can be based on electronic components which are standard items in production today. The main components of the system, illustrated in Figure 12.1, are at least one order of magnitude more compact than similar equipment now in production. Yet, they can perform the same function. System components which earlier had to be carried by heavy, specialized vehicles, can thus now be made easily portable. These advances are being made possible mainly by the modern circuit techniques such as those described in Chapters 2 and 4, and which were not available until 1974–75.

6.12.2 Command and Control Data System

Another tactical situation is illustrated in Figure 12.2, where a tactical headquarter, B, perhaps one of several operational centers, has several aids for its handling of command and control tasks. It makes use of computers, which may be located elsewhere, duplicated if necessary in vans (F) or hardened sites (E). It provides observers, officers in command, and others with small portable, perhaps even pocket sized, specialized terminals (A, D).

Various terminals and computers constitute one system, where each "member" station is specially fitted to handle one set of tasks. Some members are more general terminals, others again are centralized computers, performing various tasks for the operational personnel using their devices or stations. Each station (terminal) has built-in radio equipment and can operate without wires in buildings or outside. The radios are highly compact and use line-of-sight type propagation. Small, self-contained, automatic repeater stations (C, G) are deployed at high places in the terrain so that at least one repeater can be seen (permitting line of sight radio) from anywhere in the area to be served. Each station has communication processors in the form of microprocessors built in.

Mobile or stationary units in this system can be used anywhere within the covered area, which may be large or small (perhaps hundreds of kilometers, or within a building). The users need not worry about where the others are, and each terminal has access to powerful information handling machinery, allowing him to communicate in terms suitable to his tasks and situation.

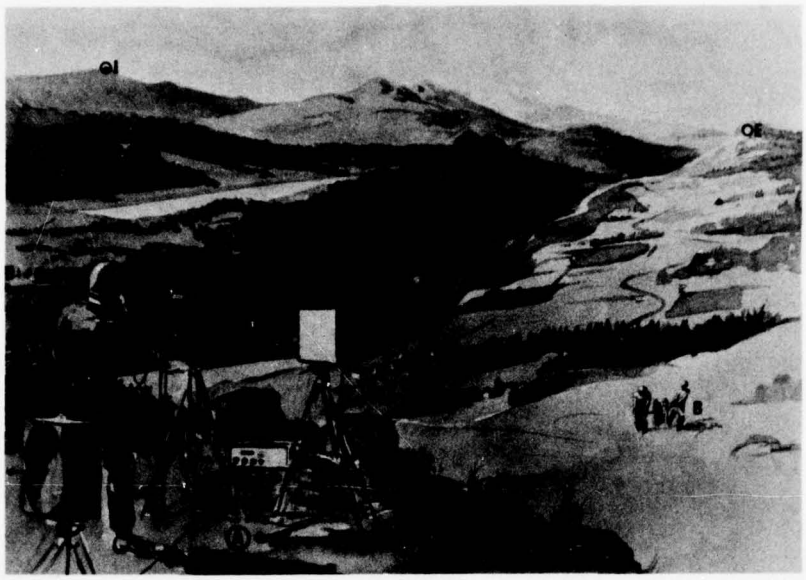
Spread spectrum modulation techniques and encryption techniques may be used for protection against jamming and for security. Radio transmissions for each terminal are very brief (milliseconds), thus conserving radio frequency usage and making detection and localizing of stations difficult. The user employs his equipment in a "dialogue" with others in the system, and always knows that his messages have been correctly received.

Computer capacity for information storage, retrieval, sorting, presentation formatting, calculations etc, is now provided by units in protected or remote places. Equipment needed at operations centers need only have the necessary screens, keyboards and possible other facilities to be directly viewed and handled by the users. Forward operations centers can thus be light, and do not have to compromise information unnecessarily. As a whole, such a distributed system has unusual potential for practical features, low cost, high survivability and flexibility.

A feature of special technical interest is the possibility for simple, automatic repeater stations. These will facilitate the use of high frequency bands, such as UHF and higher, while still maintaining good terrain coverage.

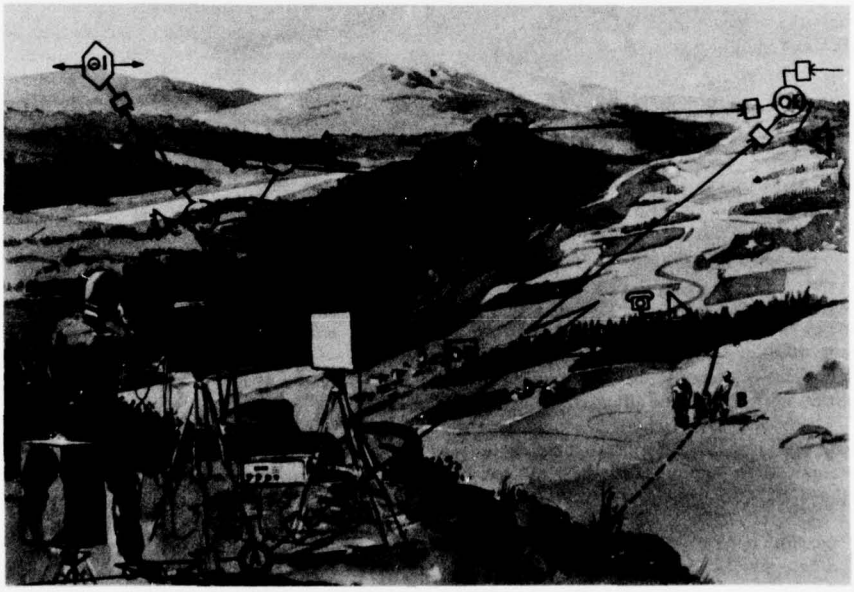
6.12.3 Fire Control Cooperation

Another tactical situation is depicted in Figure 12.3. Gun boats equipped with surface-to-surface missiles are deployed in coastal positions (C, D). Attacking enemy ships (G) would be missile targets but are out of sight from gun boats under the horizon or behind islands.



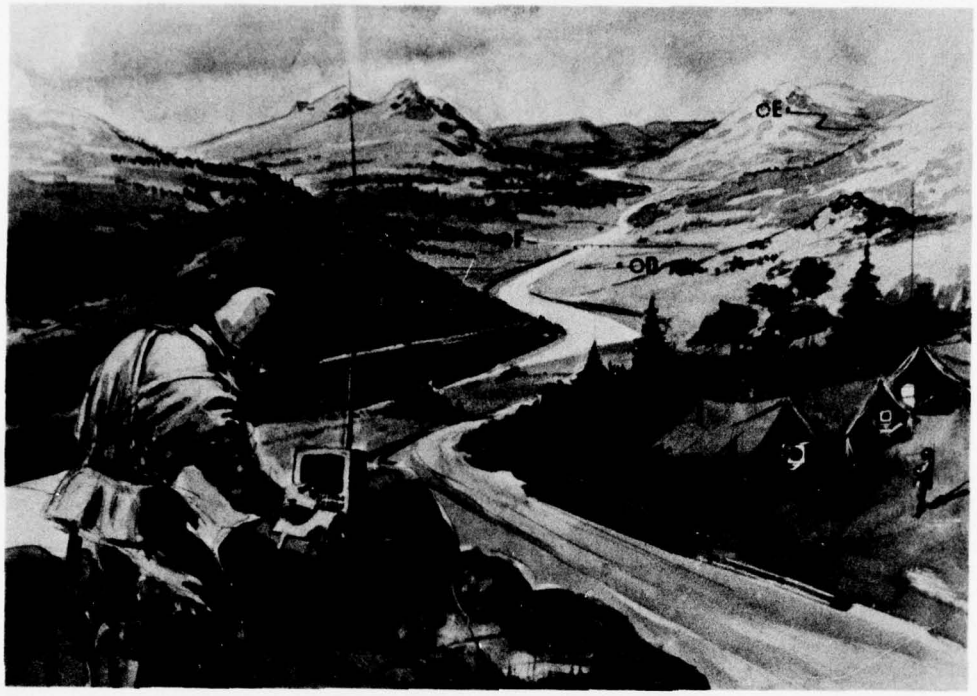
(a) Typical tactical situation

A) Communication node point under establishment
B) Cable from C
C) Headquarter
D) Access point to civil telephone system
E) Communication node and nearby headquarter
F) Microwave station cable connected to G
G) Headquarter
H) Headquarter
I) Access point to strategic communication net



(b) Schematic of mask net. Each "access multiplexer" (triangular symbol) allows up to 30 automatic telephones. All units are lightly portable. At A is shown 120-channel computer controlled switching and routing unit, and a person using service handset during establishment of radio links.

Fig.12.1 Tactical telephone system



A) Person with specialized, portable data terminal
B) Operations centre with various terminal equipment such as situation displays and other facilities for supervision, command and control
C) Automatic repeater station
D) Person with specialized, portable data terminal
E) Computer center in hardened site inside mountain, radio antenna on mountain top
F) Computer center in mobile units ("vans")
G) Automatic repeater station

Fig.12.2 Tactical radio data communication system

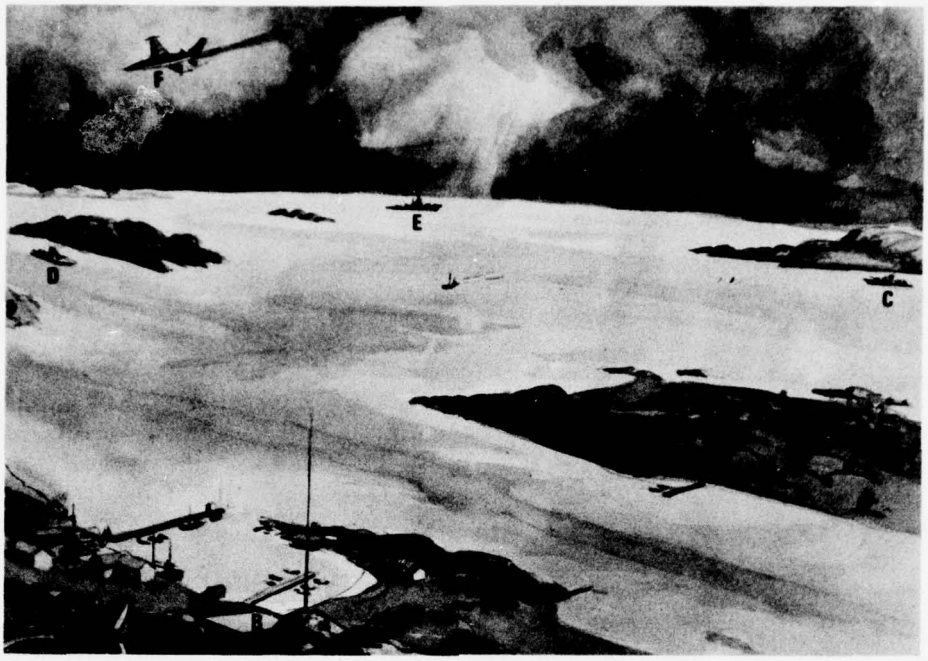
It is desirable for gun boats to be able to attack the intruding enemy, while still keeping out of his reach or at least hidden, and the attack could be made under direction from a remote command center. It is further desirable that cooperating units, which are in positions permitting observation of the enemy, viz from aircraft (F), mountains (B) or forward ships (E), can transmit observation data.

Given the means for cooperating units (B, E, F) to observe the target and to specify the observations quantitatively in some common coordinates, it is possible to operate a net where all the units mentioned communicate. Observing units would provide target data to the firing vessel sufficiently fast for practical use, i.e., without noticeable delay. Data can be transmitted to the command center and/or the gun boats and can be used by them for launching missiles even though the firing gun boat is not in a position to observe the target itself.

The entire operation could be directed equally efficiently from one of the gun boats or from a remote command center. Communications permit the use, in real time, of stored information and computer power in powerful, land-based control centers, if so desired.

In fact, the fire control system may become completely transparent, in the sense that relevant target data, other situation data and command and control information are commonly available to all who need it immediately. All the common data may be kept continuously updated directly from the sources (observers, command center etc) subject to appropriate, built-in filtering procedures for protection and other purposes, without noticeable delays.

Each user of the system, for example, a boat commander, gunnery officer, observer or operations commander, will have directly available to him all information and command facilities relevant to his task and continuously updated. As far as the information flow is concerned, the system removes the limitations otherwise imposed by time and space. Ensuing possibilities for joint operation and efficient use of limited resources are large.



A) Satellite antenna
B) Observation post (A and B need not be close to each other)
C) Fast patrol boat with surface to surface missiles
D) Fast patrol boat with surface to surface missiles
E) Own navy ship
F) Own aircraft
G) Enemy intruding naval force, out of sight from C and D

Fig.12.3 Aiming at target out of direct sight

Long distance communications, e.g., to command center, between distant ships, etc. may make use of satellite and/or other suitable transmission facilities as part of the system.

Spread spectrum modulation, powerful encryption techniques, and redundant communication paths would all be integral parts of the system, which would thus be resistant to jamming, detection, tapping and destruction.

6.12.4 Comments

The examples in the previous three sections are not indicative of systems in existence. They are meant as illustrations of what can be achieved by computer communication *techniques* which are now available or in development. They are projections of possible applications of such techniques described as seen from the potential user's viewpoint, rather than the computer specialist's. The latter may find the details outlined in the preceding sections helpful in understanding how such systems would be implemented.

It is important to realize that distributed systems such as these are only becoming feasible as a result of quite recently developed circuit technology and computer communications methods which are still in rapid evolution.

6.13 SUMMARY AND CONCLUSIONS

This discussion of communication processors and computer networks has touched upon rather wide areas of techniques and applications. The purpose has not been to present all details, but rather to give a quick survey of recent developments in the field of telecommunication which have recently become or are becoming available for practical use, as the result of advances in computer techniques.

The main impact is visible in telephone systems and in data communication systems. The field is so large that

a comprehensive treatment is impossible in a brief survey. Also, the development of computer communication techniques is very extensive. It may take unexpected routes, and may have influence in unexpected fields. Uses in telephone systems and "traditional" tasks for computers are already established realities. The techniques are in evolution, and new application areas are likely to develop.

It is relevant to consider all information as data which can be handled by computers and computer communication methods. From the initial limited scope of "using other people's computer", which has been prevalent for computer networking, the field of view should be extended to cover all information, and information handling, storage, transformation, retrieval and transmission. Information comprises numbers, text and other symbols, graphical information, speech, television and more.

Three examples of possible military applications have been described. They may be thought of as available for development in the immediate or near future. These and other applications are expected to be able to fill existing needs, thereby enhancing the efficiency of existing forces and opening for new methods, modes and tactics.

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REFERENCES

1. – *Special Issue on Computer Communications*, Proc IEEE, Vol.66, p.11, 1972.

2. – *Association for Computing Machinery etc*, Proceedings of the first ICCC, Washington, October 1972.

3. – Host: *Central Administration of Swedish Telecommunications*, Proceedings of the second ICCC, Stockholm, August 1974.

4. – No.1 ESS issue of the Bell System Technical Journal, Vol.XLIII, 5, pp.1831-2609, 1964.

5. Pirotte, A. Vitry, P. *Military Tactical Communication Network Using Pulse-Code Modulation*, Electrical Communication (ITT), Vol.62, 2, pp.125-30, (1971).

6. Lundh, Y. et al. *Node Technique*, Intern rapport E-245, Norwegian Defence Research Establishment, 1975.

7. Martin, J. *Future Developments in Telecommunications*, Prentice-Hall, Inc., 1971.

8. – *D2 Channel Bank*, Bell Syst. Tech. J., Vol.5, 8, pp.1641-765, 1972.

9. Frank, H. Frisch, I.T. *Communication, Transmission and Transportation Networks*, Addison-Wesley, Reading, 1971.

10. Frank, H. Frisch, I.T. Chou, W. Van Slyke, R. *Optimal Design of Centralized Computer Networks*, Proc. Iner. Conf. Commun., June 1969, 21.1-21.8, Networks, pp.43-57, September 1971.

11. Abramson, N. Kuo, F.F. *Computer Communication Networks*, Prentice-Hall, 1973.

12. Davies, D.W. Barber, B.L.A. *Communication Networks for Computers*, Wiley, 1973.

13. Grimsdale, R.L. Kuo, F.F. (Editors) *Computer Communication Networks*, NATO Advanced Study Institute Series E-4, Nordhoff International Publ., Netherlands, 1975.

14. Cerf, V.G. Kahn, R.E. *A Protocol for Packet Network Intercommunication*, IEEE Trans., Vol.COM-22, 5, pp.637-48, 1974.

15. Crocker, S.D. Heafner, J.F. Metcalfe, R.M. Postel, J.B. — *Function-Oriented Protocols for the ARPA Computer Network*, Proc. Spring Joint Computer Conference, pp.271-79, 16 May 1972.

16. — — *Special Issue on Interactive Computer Systems*, IEEE Proc., Vol.63, 6, pp.835-979, 1975.

17. Engelbart, D.C. et al. — *Advanced Intellect-Augmentation Techniques*, Final Report Project 7079, Contract NASI-7897, Stanford Research Institute, 1970.

18. Vallee, J. Lipinski, H.M. Miller, R.H. — *Group Communication Through Computers*, Report R-32, Institute for the Future (Menlo Park, California, USA), 1974.

19. Postel, J.B. — *A Graph Model Analysis of Computer Communication Protocols*, UCLA-Eng-7410, Computer Science Department, University of California, 1974.

20. — — *The Aloha System*, Final Technical Report B75-1, Contract NAS2-6700, University of Hawaii, 1975.

21. Lam, S.S. — *Packet Switching in a Multi-Access Broadcast Channel with Application to Satellite Communication in a Computer Network*, UCLA-Eng-7429, Computer Science Department, University of California, 1974.

22. — — Several papers on *Packet Radio* given at 1975 National Computer Conference, AFIPs Conference Proceedings, Vol.44, pp.177-261, 1975.

23. — — *Spread Spectrum Communications*, AGARD Lecture Series 58, 1973.

24. Saltzer, J.H. Schroeder, M.D. — *The Protection of Information in Computer Systems*, Proc. IEEE, Vol.63, 9, pp.1278-1308, 1975.

25. Feistel, H. Notz, W.A. Smith, J.L. — *Some Cryptographic Techniques for Machine-to-Machine Data Communications*, Proc. IEEE, Vol.63, 11, pp.1545-54, 1975.

26. — — *Draft Recommendations on Digital Transmission Systems (G 700 series)*, Document AP V-No.54 E, International Telegraph and Telephone Consultative Committee (CCITT), 1972.

CHAPTER 7

HIGH PERFORMANCE DIGITAL SIGNAL PROCESSORS AND APPLICATIONS

by

J.M.Frankovich

7.1 INTRODUCTION

The uses of and needs for signal processing in tactical military systems has increased enormously in recent years. All kinds of surveillance, fire control, guidance, communication, and other systems require the processing of signals collected by sensors before these returns can serve a useful decision or control function in the system. Ever since World War II, there has been a tremendous growth in the development of closed loop systems which require real time, high performance processing of such signals. In this context, high performance is taken to mean large volumes of data passing at high rates through a complex processor. Recent and projected development of military systems indicate the need for continued increases in these three parameters of volume, speed and complexity.

A common example of the kind of system under discussion here is a radar in which the return signal must be filtered in some manner in order to obtain the desired information about the target. In the past such signal processing systems were almost always entirely realized with analog hardware. In this chapter, the emphasis will be placed on the opportunities for using digital techniques involving the newer types of integrated circuit technology discussed in some of the earlier chapters.

The practical value of using digital technology here arises from the possibility of realizing systems at a lower cost than can be realized with analog equipment, and which have a greater flexibility and an adaptability to a wider variety of parameters (and changes in them). This has become particularly true in recent years as the development of higher performance and more compact and reliable circuit technologies has permitted the design of higher speed and higher bandwidth signal processors. A further advantage of digital over analog signal processors is the reduction in signal to noise levels in the processor output. In an analog processor each processing element usually significantly and measurably degrades the S/N ratio of the information passing through it, whereas in a digital system this effect can be substantially eliminated by the simple mechanism of carrying enough digits in each element.

In the following discussion the organization of typical systems will be explored in order to illustrate the areas in which digital technology can be used. Emphasis will be placed on the organization of radar systems in order to indicate the impact of the availability of fast logic and large fast memories on system design. However, smaller and/or lower performance systems can also be effectively realized using similar logic.

7.2 BRIEF OVERVIEW

Military signal processing systems usually employ sensors which receive acoustic, electro-magnetic, or optical signals. Some systems are active, as in the case of most radar and communication systems which both transmit and receive signals. Others, such as some sonar and some optical systems, passively receive signals.

In a digital signal processing system, the returned signal is digitized at some point after the sensors by analog to digital converters. A typical system passes the digitized signal through a sequence of processing and buffer memories. The result may be presented to an operator with or without the intermediary of a large data processor. In an active system, as shown, one or the other of these would then cause additional signals to be transmitted, usually by the same sensor.

In many systems, such as air traffic control radars, these transmissions may occur at a regular rate and the receptions are interleaved at the appropriate times. In more complex systems, however, the type and the interpulse period of the transmission may be strongly dependent upon the nature of the information extracted by the signal processor from the previous or earlier received signals and there may be a strongly interactive scheduling effect upon the total activity and work load of the system. In such systems, the use of digital techniques throughout the signal processing chain permits the values of the system parameters to vary widely, thus gaining increased flexibility.

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In all such systems, the desired information lies in some frequency band to which the sensor must be tuned. All signal processors employ a filter which is matched to this incoming signal band. In some cases the band is moved so that it is centered at baseband and in others only a bandpass filter is used. In either case more sophisticated systems use filters which are closely matched both to the characteristics of the originally transmitted signal and to the characteristics of the target.

The output of such a matched filter is then usually passed through a succession of processors. In a radar or sonar system we are usually concerned with detecting a target and determining some of its characteristics. In such cases the next processor is typically a detection processor which determines whether there is sufficient energy in the return to exceed some threshold. This threshold may be predetermined or itself determined in a different fashion from the original return at the output of the matched filter.

In a simple system, the output of this processor would be characterized either as a point or a distributed target and this output would be displayed to the system operator. In a more complicated system, the threshold output of the detection processor would be presented to yet another processor wherein various computational algorithms would be performed which yield such target metrics as range, velocity, acceleration, and direction angles. In addition, various target characteristics might also be determined such as, in radar systems, the target length and cross-section, in sonar systems, the frequency dispersion, or in MTI systems, the scintillation and wind shear. In virtually all such systems, the output of this signal processor is then fed to a data processor of some sort which can range from a human operator to a large data processing computer. This processor, of whatever sort, would perform target recognition, tracking, or other pattern recognition functions and determine subsequent control actions.

In communication or guidance systems, various commands, data, or other information needs to be extracted from the received signal. This information is frequently coded in a complex fashion in the waveform and considerable signal processing may be necessary in order to extract it. In these systems the output of the filtering operation is fed to a decoding processor which deciphers the received message[1].

Several parameters can be used to characterize such signal processing systems. One is the bandwidth W of the input channel signal to be processed. This may range from a low of 10 Hz in sonar (or even less in seismic[2]) systems to more than 10 MHz in radar systems. Another parameter is the duration T of the signal. The product TW, or time-bandwidth product, is characteristic of the "dimensionality" of the signal and is a fundamental parameter. In typical systems this may range from less than 10 to 10,000 or higher. Another, less obvious, parameter is the amount of time allowed between the signal reception and the response to it. This time reflects the environment in which the signal processor operates and may be as short as a few milliseconds in radar systems to several seconds in sonar systems. The number of input channels may also be a parameter when multiple polarization or monopulse error signals can be received. These parameters and others together determine the speed at which the signal processor must operate and the volume of data which it must process.

7.3 APPLICATIONS OF NEW IC TECHNOLOGY

The various subsystems in a signal processor lend themselves to different techniques in the exploitation of new digital IC technology. The filter usually is a special digital processor tailored to a specific, but nonetheless broad class of waveforms, possible targets, and operating speeds. The detector is another special processor although the variety of detection algorithms seen in a particular system is usually rather limited. The algorithm processor may be a special or a general purpose computer, depending upon the application. A decoding processor may be a general purpose computer but is frequently a specially arranged sequence of tapped shift registers which invert the process used to generate the code in the transmitter.

Buffer memories are usually interspersed between processors and provide two functions. First, they collect data from one stage and hold it until the next one is available. Second, and perhaps more important, they permit the redimensioning or reformatting of the data as it flows through the system.

The data flow through a signal processor can be seen to be basically sequential. If buffer or register memories are used to subdivide stages so that successive elements are working on successively earlier returns, then we call the processor pipelined sequential. Depending upon the application, this may require that the intermediate memories be doubled buffered or interleaved in operation. Sometimes, in order to gain additional performance, some stages of the processor may be replicated so that they can operate in parallel on different parts of the signal. Thus, the signal processor may be parallel and/or pipelined sequential. The signal processing algorithm itself may cause the volume of data processed at different stages to vary and this effect may determine the need for introducing parallelism in an otherwise sequential processor.

7.3.1 Filters

Simple digital filters can in principle be realized as a combination of delay memory elements and gated adder circuits[3]. A typical recursive filter with q poles and p zeroes can be realized by forming the sum of products of

$p + q + 1$ tabulated filter coefficient values with the $p + 1$ previous input data values and the q previous filter output values. The data values can be delayed in memories and multiplied by the filter coefficients which can be obtained from coefficient memories. These can be fixed (ROM), variable (RAM), or sequential (disc, drum, or shift register) memories. The possible realizations can also reflect various degrees of parallelism or pipelining, depending upon the desired matching of circuit and processor performance.

In the simplest form of the filter, all the $p + q + 1$ values of input and output values would be held in a shift register delay memory. Each value would be successively read out from (and reinserted into) the memory, multiplied by the proper coefficient, and the sum accumulated. These operations would be scheduled so that the final output result would replace the oldest filter output value in the memory and a new input data value would replace the oldest input value. Then the process would be repeated to obtain the successive filter output values at a cost of $p + q + 1$ shifts, multiplies and adds for each output value. If performance time requirements permitted, each multiplication could also be realized by an inner loop of d additional arithmetic shift and adds, where d is the number of digits in the coefficients.

Another form of computation which is useful for matched filtering, spectral analysis and Doppler filtering is the finite digital Fourier Transform (DFT) (Ref.4). A matched filter can be realized, for example, by a DFT, followed by a multiplication, and by another DFT. Instead of processing a continuous flow of data points, a DFT deals with a block of N data points at a time. This formulation requires a $2N$ word sine and cosine coefficient memory and some N^2 operations (multiply and add) in order to form the transform of each block of N data samples. This is acceptable for small values of N, but since N must exceed the time-bandwidth product and usually equals $2TW$ for continuous data streams, the amount of computation rapidly becomes unmanageable as N increases.

The radix-R "fast" Fourier Transform (FFT) algorithm is used to reduce the number of computational operations from N to $(N/R) \log N$ (Ref.5). These operations, which are sometimes called "butterfly" computations, are simply an R point DFT. The complexity of the operation depends upon the radix-R of the logarithm. For example, when $R = 2$, it is an addition and a subtraction. Associated with each operation are $R - 1$ multiplications. In the design of an FFT processor, major emphasis is usually placed on fast execution of these operations and multiplications. The principle difficulty then remaining in designing an FFT processor is one of scheduling the data flow so that the operations are performed in the sequence required by the nature of the FFT algorithm. The FFT lends itself to straight-forward pipelined realizations[6] which permit very high data clock rates. In these, the data is manipulated in multiply-switched delay memories between the successive computational elements which perform the operations. In recent years, large filters with very generalized capability have been implemented with the FFT algorithm and have been used in a wide variety of applications.

Many specialized MSI IC packages are available which simplify the design of such logic. The TTL 74181 and ECL 10181 are four bit multiple arithmetic and logic function packages which have proven very useful in the design of adder, shifter, and multiplier arrays. In ECL there is also the 10287 package which is useful for high-speed adder and multiplier arrays[7]. Many design examples which employ these packages are available in the literature[8].

In both forms of the Fourier transform, the coefficients are usually precomputed and held in a readily accessible storage. Depending upon the nature of the applications both ROM and RAM packages, which can be found in a broad variety of speeds and capacities, have found use as coefficient memories. In high data rate radar applications it is frequently necessary to multiplex or interleave these memory packages in order to obtain performance speeds which match those achieved with available high-speed arithmetic logic packages.

In pipelined processors, delay memories for the data can be realized either by RAM's in which the data addressing is manipulated in correspondence with the indices, or by true shift register memories in which the data is actually moved sequentially in order to maintain correspondence with the indices. Both kinds of memory chips are available in TTL technology. In ECL, high-speed RAM's are more likely to be used simply because of the lack of availability of large shift register packages. The newer CCD packages permit block-addressed sequential accessed large capacity memories to be realized at a comparatively low cost when these characteristics are required.

Digital filters are frequently designed as special purpose hardware boxes which incorporate the techniques just described. This filtering function can also be realized in a programmable machine (which performs other functions also)[9] when the system requirements can be met with such a machine[10]. This is particularly true if the signal processing can be done in non-real time.

7.3.2 Data Buffering Memories

An important question in the design of any digital signal processor is whether the data are collected by the A/D converters and processed at a steady time synchronous rate, or whether the data collection is intermittent or mismatched in some fashion to the processing rate so that an intermediate input data buffer memory is required between the A/D converter and the filter hardware. This occurs frequently when there is more than one sensor and only one filter, as in the case of monopulse radars which have a sum input channel and two error input channels. Here, data can be collected for a short period of time from all channels simultaneously and then processed

separately and sequentially through a filter. Only the sum channel is passed through the detector, but all three channels are recombined on a point by point basis in order to determine the radar antenna pointing angle errors for each target.

In these cases, both the input data buffer memories and the intermediate, post-filter data buffer memories can become very large. The write speed for the input memory must also match the sampling clock rate of the A/D converter.

If, for example, the radar with three input channels had a bandwidth of 1 MHz, a waveform 1 ms long (i.e., TW = 1000), a range window of 1 ms (150 Km), and was sampling the data at the Nyquist rate (1 MHz), then 6000 complex data points would be collected during each return at a rate of three megasamples per second. Typically, however, there would be an interpulse or inter-return period 10 or more times longer than the pulse length so that the sampled data can be accepted by the filter at an average rate less than 300 KHz. Thus, there is a very distinct advantage to collecting all of the sampled data in an input data buffer so that the filter and successive parts of the signal processor can be operated more or less continuously at a substantially lower clock rate.

In this example, such an input buffer could be realized compactly and at low cost with MOS 1 K bit or larger memory packages. If the sampling rate were higher or there were more input channels, then TTL or ECL memory packages can be used. With current ECL 1 K bit packages and 8:1 multiplexing, peak sampling rates of over 100 MHz could be accommodated, but because of the resulting memory size this sort of design would be efficient only with a TW greater than 8000. Nevertheless, with present A/D performance levels it is possible to collect large quantities of digital data at high rates for later, slower filter processing. Of course, if the requirement is for collecting large quantities of low data rate samples, then the MOS, CCD or newer IIL technologies would be preferred.

In many signal processing systems the need exists for large intermediate data buffer memories. For example, the original input signal may be passed through different Doppler filters at successive times in order to permit a two dimensional range-Doppler algorithm to be used. In this case, the volume of data is expanded by the number of Doppler frequencies, although the input clock rate is unchanged.

Thus, in the previous example, if we consider only the sum channel and four Doppler frequencies, then the original data set would expand from 2000 points before Doppler filtering to 4000 points after filtering. Again, with the same assumptions as above and ignoring the error channels, this intermediate buffer memory would operate at less than 400 KHz for either reading or writing, or a total of 800 KHz for the combined memory operations.

These speeds and these memory capacities are certainly easy to achieve with MOS packages, but in higher performance large signal processing systems it becomes difficult to achieve the desired performance even with ECL packages. In such systems it becomes desirable to use double buffered memories (i.e., two separate memories which isolate the reading from the writing operations) and to try to take maximum advantage of whatever peculiarities may exist in the way that the particular signal processing algorithms require the memories to be accessed.

Another aspect of buffer memories designed for these sorts of applications is the different accessing requirements for reading and writing. For example, the input buffer memory for each channel of input data coming from the A/D converters must be accessed in strict time sequence when the data is being inserted into the memory. But if the filter is realized by a radix-R FFT processor, then the data must be read out in R multiple parallel streams. This places another burden on the design of the IC package multiplexers in the memory which adds to the limitations on the memory performance. Similar problems can exist in other of the buffer memories in the system. Thus, the design of the signal processor can require a major emphasis on the design of the buffer memories.

7.3.3 Detection Processors

The detection processor in a signal processing system usually performs the function of reducing the volume of data which must be processed by later elements in the system. This is done by comparing the filtered signal with a threshold value; data which exceeds this threshold is then marked in some way and then passed on to the next stage in the system. Depending upon the system, the data which does not pass the threshold may or may not be also passed along. Frequently, the threshold is itself computed in some fashion from the signal by applying a simple filter, e.g., a moving average or a weighted window. If the signal is a complex number, then the magnitude must also be computed.

As in the case of the filter, this processor is usually realized by special hardware which incorporates a small amount of delay and coefficient memory and arithmetic logic. If required, more special hardware might be used to compute the magnitude of the data and compare it with the threshold. In some systems additional logic must be provided in order to perform different threshold functions upon different signal returns. This can lead to complicated switching arrays in order to accommodate the high data rates of the system. It is here that some of the new data selector and multiplexor IC packages can be used to simplify the data path switching problem.

7.3.4 Post Processors

Whether or not a detection processor is used, the output data from the filter is usually processed more extensively in a post processor. Here more complicated algorithms are performed upon the (usually) considerably reduced volume of data. Thus, for example, when a target is detected, the antenna pointing angle error might be computed or an interpolation might be performed to determine more precisely the target metrics in range and/or Doppler frequency space.

Calculations of this sort usually involve evaluation of a variety of difference equations which use only the data points in the immediate neighborhood of the detected target. If there are only a few such equations then it is sometimes expedient to build a small, special-purpose device. Frequently, however, a more sophisticated radar system will require a variety of evolving algorithms and so it becomes desirable to use a small, but fast, general purpose computer.

On the other hand, in communications[11] or speech processing[12] systems, long sequences of filtering data are processed in order to extract the desired information. Such systems usually apply only a limited set of computational procedures, hence the post processor would ordinarily be realized by special purpose hardware. Even so, these procedures are also frequently so complex that it becomes easier to program them in a computer.

There are many general purpose short word length (approximately 16-bit) "mini" computers on the market which can execute instructions at about a 1 MHz rate. These have proven satisfactory for some systems since long word lengths are usually not required in signal processing applications. Some "specialized" general purpose minicomputers have also been developed for signal processing applications. Instruction rate speeds higher than 10 MHz have been achieved using ECL or Schottky TTL logic. The emphasis in these machines has been upon achieving high multiplier speeds, since multiplication is a frequent operation in these computations.

There is also a need for a high-speed input/output system because a rather large amount of data must be moved through these computers. Machine designs have been proposed which use multiple processors bussed together so as to reduce both the peak-computational and input-output loads on the system[13]. In the next section, we shall discuss the design of some of these computers more extensively.

A special kind of post processor is required when the detection processor encounters a large number of targets or clutter within the volume of space being searched by the sensor. In such cases, the post processor might be simply required to define the boundaries of the region, or it might be expected to correlate data returned from several successive search pulses, perhaps with different waveforms, and to determine which, if any, of the detections correspond to a real target. This kind of computation requires that the post processor collect large quantities of data which are processed over a more extended period of time using more complicated algorithms.

In many systems these computations are left for the large, general purpose major data processor in the signal processing system. This computer, however, tends to be loaded to capacity by its responsibility for overall system control and management. Hence it becomes advantageous to design a high performance post processor which can help reduce the volume of data sent into the major data processor. For this reason the general purpose post processor might include large fast IC memory arrays as well as a high-speed arithmetic element.

7.4 DEVELOPMENTS IN PROGRAMMABLE COMPUTERS FOR SIGNAL PROCESSING

In recent years a number of commercially available computers have become available which are intended to be specially suited for signal processing applications. In addition, limited production militarized and research machines have also been developed. All of these machines have tended to have short word lengths (approximately 16 bits), as do most "mini" computers. The distinguishing features, however, tend to be the use of special architectures to achieve the fastest possible computation rate in highly coordinated memory and arithmetic units.

Commercially produced signal processor computers began to be introduced in the late 1960's. These used early designs of MSI TTL memories and SSI logic to realize cycle times as short as 300 ns. Although the available IC memory packages were limited in size, they were augmented by core memories to achieve larger capacity. By suitably scheduling the flow of data and programs through the fast memories it was possible to perform signal processing far faster than with contemporary commercial general purpose "mini" machines. One important feature was the use of register file IC packages for multiple (up to 32 or more)[14] accumulators. This feature permitted many operands to be kept on hand rather than stored in and retrieved from memory, and is indicative of how early MSI IC developments were exploited for signal processing uses.

In recent years the design of other commercially available signal processing computers has reflected the availability of more highly integrated circuit packages. Recent architectures have also divided the machine into several sections in order to obtain faster, paralleled operations. For example, in one later machine design[15] an input-output section manages the data flow and the operation of the other two sections, an arithmetic section performs the actual signal processing computations for either filter or post processor algorithms, and an index section manages the data

manipulations within a coordinated network of separate, small IC RAM's and ROM's which contain the various programs and data blocks. The arithmetic section in particular has a parallel pipelined byte rather than word structure in order to realize the desired compromise between speed and economy. All of the logic is TTL with some Schottky elements. A complete "butterfly" (a two point DFT) can be performed in one microsecond in parallel with the input-output data flow. In another commercially available machine this butterfly can be done in one-half microsecond.

The development of MSI ECL logic and memory packages has lagged somewhat behind corresponding events in the TTL area. Early ECL machines were mostly found in the large or "super" computer area[16] and were characterized by very high computing speed. By necessity these machines used mostly discrete or SSI IC components. More recent designs use both MSI and LSI components. As an aside, it is interesting to note that these machines, and the early signal processor machines just described, are essentially single instruction stream – single data stream machines in which computing power is achieved primarily by the use of high-speed, highly integrated components as well as by architectural innovations. In the later signal processor machine, the processing program functions are divided so as to realize a multiple instruction stream machine, i.e., the control type instructions in a program loop are run concurrently in a separate processor from the arithmetic type instructions. As mentioned before, this again represents the exploitation of memory chip developments, particularly for use as register files.

In the FDP research computer[17] developed at MIT Lincoln Laboratory a different approach was taken to obtain high signal processing speeds. Here a four way parallelism in the arithmetic element and matching parallel access to data memories yielded a single instruction stream-multiple data stream machine with very high signal processing performance in a small computer. An instruction time of 150 ns was achieved using primarily SSI ECL packages for logic and MSI packages for memory.

The LDVT computer[18], a more recent design at Lincoln Laboratory which uses a large percentage of MSI ECL logic packages, is also intended for signal processing, particularly real-time speech applications. Separate program and data memories, realized with LSI ECL packages, are accessed in parallel to achieve a 55 ns effective instruction time. This single instruction stream – single data stream machine has a high-speed multiplier, realized with MSI packages, and an instruction code designed for high performance signal processing applications. The parallelism in arithmetic computations used in the FDP and other machines to achieve high performance in FFT calculations could be dispensed with and the result was a reduction in size and cost both in hardware and programs.

Many standard general purpose mini and larger computers have been used in various parts of signal processor systems. These efforts can be successful when the performance requirements are easily met. When they are not, the performance of the computer can be enhanced by attaching a special purpose box as a peripheral device. The multiplications and additions corresponding to the filter calculations can be performed in this peripheral without the compromises usually required for this hardware in the general purpose machine. Such a box can make maximum use of available technology to achieve high-speed and to accommodate the word lengths and data formats required for the application.

Generalized boxes of this type have been produced commercially. Early in the history of mini-computers, "array" processors of this type became available. This kind of configuration could perform matrix as well as filter calculations rapidly and efficiently. If the host computer for such a box does not directly enter into the primary signal data flow of the processor then we essentially have a specialized signal processor where the host computer simply becomes a control computer. This is a typical situation for the case where maximum performance is desired and a flexible operator control interface is implemented via a computer.

7.5 RELATED DEVELOPMENTS IN DIGITAL SIGNAL GENERATION

In a radar or similar system the transmitted signals are usually generated by some form of analog hardware specially tuned to generate exactly the waveform desired. The filter in the signal processor must be carefully matched to the waveform actually transmitted. In systems where a large number of different waveforms are needed, a cumbersome array of special hardware is required. Such systems in many cases, present a difficult maintenance problem.

It is possible to use digital techniques to synthesize a waveform at baseband frequency and to use the same digital hardware for many different waveforms[19]. In the simplest design, the time samples of a waveform are stored in a memory. These can be read out at the required rate at the required time and then passed through a digital to analog converter and a smoothing filter before being used to modulate the high carrier frequency.

This approach exploits the availability of large capacity IC memory packages. For example, a complex 1 MHz bandwidth waveform with a duration of 100 microseconds and sampled at twice the Nyquist rate would require a memory of 200 complex words and would operate at a 2 MHz rate. Thus a collection of ten or more waveforms with similar time-bandwidth products could be stored in an IC memory of only a few thousand registers. This can easily be realized in MOS, TTL or ECL technology. The implementation would depend upon the maximum sampling

frequency desired as well as the capacity. ROM's could also be used if there is no requirement to alter the collection of waveforms.

Another technique is to construct the waveform samples by some computational algorithm in a special or general purpose computer. CW and LFM waveforms are frequently used in the substructure of more complex waveforms and can be easily generated by simple recursive algorithms for the phase function. As in the case of filter algorithms, these techniques require simple shift, add, and multiplier logic and a small amount of memory. Thus similar approaches can be used to generate as well as process real time signal samples. The signal generator need not necessarily operate at real time rates since its output can be stored in a single waveform buffer memory which is read at real time rates.

7.6 SUMMARY AND CONCLUSIONS

The uses of digital techniques in the signal processing area represents a significant advance. Not only do they permit an increase in both computational precision and long term stability but they permit the realization of filters and algorithms which would be awkward or impossible with analog techniques.

Digital systems can also be much more cost effective. This is becoming increasingly true as logic and memory integrated circuit technology become more advanced. Low power, densely integrated MOS and ILL chips will permit compact realization of complex low bandwidth processors and increasingly complex and fast bipolar packages will allow the development of large high performance processors. A digital system will also tend to have a longer useful lifetime because of its greater flexibility and adaptability to changes in system requirements.

Rapid developments can continue to be expected in the digital signal processor area since most of the hardware components and requirements are similar to those of the general purpose digital computer field. There is the interesting possibility of employing multiple technologies to take advantage of emerging CCD and SAW (surface acoustic wave) device developments[20].

It is also interesting to note that the simplification in computational complexity of many filter and post processor algorithms, most notably in the realization of the FFT algorithm, has played a significant role in the development of digital signal processors. Without these advances many digital processes would have required a complex realization and would not have been able to compete effectively with analog systems.

REFERENCES

1. Dixon, R.C. — *Spread Spectrum Systems*, John Wiley & Sons, 1976.

2. Briscoe, H.W.; Fleck, P.L. — *A Real-Time Computing System for LASA*, AFIPS Conference Proceedings, Volume 28, Spring Joint Computer Conference, pp.221-228, 1966.

3. Rabiner, L.R.; Gold, B. — *Theory and Application of Digital Signal Processing*, Prentice-Hall, 1975.

4. Blankenship, P.E.; Hofstetter, E.M. — *Digital Pulse Compression via Fast Convolution*, IEEE Transactions on Acoustics, Speech, and Signal Processing, Volume ASSP-23, No.2, pp.189-201, April 1975.

5. Gold, B.; Bially, T. — *Parallelism in Fast Fourier Transform Hardware*, IEEE Transactions on Audio and Electroacoustics, Volume AU-21, No.1, pp.5-16, February 1973.

6. Groginsky, H.L.; Works, G.A. — *A Pipeline Fast Fourier Transform*, IEEE Transactions on Computers, Volume C-19, No.11, pp.1015-1019, November 1970.

7. Pezaris, S.D. — *A 40 ns 17-Bit by 17-Bit Array Multiplier*, IEEE Transactions on Computers, Volume C-20, No.4, pp.442-447, April 1971.

8. Baugh, C.R.; Wooley, B.A. — *A Two's Complement Parallel Array Multiplication Algorithm*, IEEE Transactions on Computers, Volume C-22, No.12, pp.1045-1047, December 1973.

9. Martinson, L. — *A Programmable Digital Processor for Airborne Radar*, Record of IEEE 1975 International Radar Conference, IEEE Publication 75 CHO 938-1 AES, pp.186-191.

10. Daly, R.H.; Glass, J.M. — *Digital Signal Processing for Radar*, EASCON 75 Record, IEEE Publications 75 CHO 998-5 EASCON, pp.215A-G.

11. — Dixon, op. cit.

12. Hofstetter, E.M. et al. *Vocoder Implementation on the Lincoln Digital Voice Terminal*, EASCON 75 Record, IEEE Publications 75 CHO 998-5 EASCON, pp.32A-J.

13. Lundh, Y.G. *Multi-Processor Systems for High-Capacity Signal Processing*, Record of International Conference on Computer Communications, pp.325-329, Stockholm, Sweden, August 1975.

14. Graham, D.N. *FFT Algorithm*, Proceedings of the 1971 IEEE International Computer Society Conference, IEEE Publications, No.71C41-C, pp.11-12.

15. Allan, J. *Computer Architecture for Signal Processing*, Proceedings of the IEEE, Volume 63, No.4, pp.624-633, April 1975.

16. Thornton, J.E. *Parallel Operation in the Control Data 6600*, AFIPS Conference Proceedings, Volume 26, Part II, pp.33-40, Fall Joint Computer Conference, 1964.

17. Gold, B. et al. *The FDP, A Fast Programmable Signal Processor*, IEEE Transactions on Computers, Volume C-20, No.1, pp.33-38, January 1971.

18. Blankenship, P.E. *LDVT: High Performance Minicomputer for Real-Time Speech Processing*, EASCON 75 Record, IEEE Publications 75 CHO 99805 EASCON, pp.215A-G.

19. Eber, L.O. Soule, H.H., Jr *Digital Generation of Wideband LFM Waveforms*, Record of IEEE 1975 International Radar Conference, IEEE Publication 75 CHO 938-1 AES, pp.170-175.

20. Hartmann, C.S. et al. *Programmable Transversal Filters Using Surface Waves, Charge Transfer Devices, and Conventional Digital Approaches*, Proceedings of the International Specialist Seminar on Component Performance and Systems Applications of Surface Wave Acoustic Devices, IEE ISBN 0-85296-117-0, pp.102-114, September 1973.

CHAPTER 8

TRENDS IN AEROSPACE COMPUTERS

by

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8.1 INTRODUCTION

This report is concerned with surveying the use of general purpose digital computers in the NATO tactical situation. This chapter covers those applications which are traditionally carried out in the airborne situation as well as those where advancing technology has made an airborne solution viable. In the latter case it is generally the reduction in physical parameters which has made possible control and data-processing tasks, which were previously carried out in a ground installation, possible in an aircraft, thus improving tactical effectiveness.

The division of airborne computing tasks into the two classifications of control and data-processing is important[2]. The first class covers essentially real-time situations where the computer is a component in a complex control situation. In the second case the computer system, including peripherals, is the entire system performing the required functions. These two application areas require differing considerations to be applied to the design and selection of a digital computer.

The most important difference between ground and air based systems is the environmental/physical conditions prevailing in an aircraft. Thus the first part of this chapter looks at this problem and how technological developments are improving the situation. This is followed by consideration of how far advances in computer architecture, technology, memories and software, described in previous chapters, are applicable to airborne systems. Finally some applications are considered and problem areas highlighted.

8.2 TRENDS IN AEROSPACE COMPUTERS

8.2.1 Physical Requirements

A major difference between airborne and ground based computers are the stringent physical requirements in the aircraft environment. Thus the physical volume, shape and weight are major design constraints. In the last decade the increasing availability of complex integrated circuits together with high density packaging technologies has resulted in an order of magnitude improvement in weight and volume. These reductions have not been accompanied by performance losses, rather the "computing power" has considerably increased. Thus a typical aerospace computer has increased its instruction throughput over a decade by more than an order of magnitude.

The first improvement in physical characteristics came with the introduction of silicon integrated circuits, an even greater impact has been made with the introduction of large scale integration (LSI) devices, both bipolar and MOS. It is now feasible to fabricate a fairly complex processor on a single LSI chip although the result is not comparable in terms of computing power to currently available processors of a more conventional type.

8.2.2 Environmental Requirements

The environment to which an airborne computer is subjected can vary from a temperature and pressure controlled equipment bay to an engine mounted situation where very high temperatures and vibration levels are experienced at atmospheric pressure. Two major problems then became apparent, the removal of the heat generated within the computer to some suitable sink and the construction of the computer to withstand high vibration levels. In addition the equipment may be subjected to high electromagnetic fields, humidity, various liquids and generally rough handling.

In an equipment bay air is generally available for cooling purposes thus allowing a unit to be convection cooled, in some cases air is available at pressure for forcing through the unit.

In these cases the thermal problem is the efficient transfer of heat from the device to the convection cooled wall or finning. Minimising this temperature gradient then defines the maximum allowable cooling air temperature for an acceptable device temperature. Techniques in use involve metal ladders inserted between devices and the interconnecting

board, high thermal conductivity substrates for interconnection and metal cored circuit boards. Use of these methods enables temperature gradients of 20–40°C to be achieved in computers. Assuming maximum device temperatures of 125°C it is therefore possible to operate computers in ambients of up to 100°C.

The other major problem area is in the mechanical design of the computer to meet the vibration and acceleration requirements of the airborne environment. It is desirable to keep component g levels to below 100–120 g. The vibration level to which the unit is subjected then defines the necessary degree of damping which must be incorporated.

8.2.3 Reliability

The reliability of airborne computers has improved considerably with the introduction of large scale integration and packaging techniques, however it is very difficult to compare mean-time-between-failure (MTBF) figures unless the basis of the calculations is consistent. Reliability can be improved by utilising high reliability components which have been through a burn-in procedure, however this increases component procurement costs. Reliability can also be improved by reducing the number of components and interconnections in the system and by improving any adverse operating conditions, such as ambient temperature. The resulting design involves therefore a number of trade offs to be made which are dependent on the requirements of a particular case.

8.2.4 Computing Capability

The trend over recent years has been towards more specialised instruction sets in aerospace computers, aimed at specific classes of use. This trend has been accelerated with the growth of microprogrammed processors, a technique which allows different instruction sets to be implemented in common hardware. Early processors had their instructions defined by hardwired logic, and, with some exceptions, were standard type sets applicable to any type of problem. The availability of inexpensive, high density, semiconductor memory has opened the way to microprogrammable processors. The instructions are here defined by the contents of a microprogram memory, in general the operation code is used as the memory address and the resulting data word sets up the necessary data paths in the processor and defines the operation of arithmetic and logic units. Simple instructions may require only one microprogram word but this may be extended for more complex instructions. A further variable is the width of the microprogram word, and hence store. This may be fairly small, 16–24 bits, or may be as high as 128 bits. The shorter this word length then the more complex is the hardwired decoding logic required and the less flexible is the processor. The shorter word length does however make microprogramming easier.

A microprogrammed processor does enable the same processor hardware to be provided with different instruction sets applicable to different applications. Examples here are graphics processors where instructions to draw lines or circles are provided, and to generate alphanumerics. Similarly instructions to implement vector or matrix algebra may be implemented.

A further development is the implementation of 'high level' instructions in microprogramme. These high level instructions could be required system functions, for example function generation, integration or limit checking.

This concept has been used successfully in the implementation of real-time control of an aircraft sub-system with attendant savings in programming and debugging time.

An important contributor to the power of a processor is the speed at which instructions are executed. Two developments have made an impact, the use of higher speed logic devices, such as Schottky, TTL and ECL, and the development of processor architectures where an increase in the number of parallel operations increases speed. The logic devices have been described in Chapter 2 and most have been applied to airborne processors. Due to the more stringent power and volume requirements in the airborne environment however, Schottky TTL has tended to be used in preference to ECL where speed has been of importance.

Modern processors employ a number of techniques for increasing instruction throughput, for example pipelining and overlapping. The conventional approach was to read an instruction from memory into a register in the processor. This instruction was decoded, the necessary data paths set up and the instruction executed. With a pipelining system a number of instructions, for example 2 or 3, will be at different stages, with a core memory system one instruction will be in the instruction register and the next in the memory data register. The memory will be setting up the address of the next required instruction and, in the case of an interleaved memory, the previous instruction restore cycle would be underway. A processor employing instruction overlap may have two or three instructions at different stages of execution. For example in a microprogrammed processor the first instruction would be moved from arithmetic unit to general register while the second is being propagated through the arithmetic unit, the third is being transferred from the general registers and the fourth is setting up the next microprogram address.

These techniques have resulted in airborne processors with throughputs an order of magnitude greater than seven to ten years ago.

An advanced modern computer may have 75 to 150 instructions and these can be executed by the processor at speeds in excess of 10 MHz.

8.2.5 Memories

The provision of suitable memory poses many problems in an airborne system. A system which is to be produced in quantity usually has a requirement for fixed memory for programme and fixed data plus a scratch pad memory for storing transient data. The requirements for the fixed store are reliable retention of data in both the powered and unpowered states, economy in mass production and minimum requirements for volume and electrical power. These requirements are best met today by semiconductor read-only memory. The problem is the development and pre-production stages where many changes of the memory may be expected. The optimum solution would be a memory that was:

- Read only but electrically re-programmable,
- Non-volatile,
- Non-destructive readout.

Semiconductor memories that meet these requirements are becoming available, for example P-channel MNOS memory where a charge is trapped at the interface of a silicon dioxide layer and a silicon nitride layer which form the gate insulation of an FET transistor. Data is stored by applying a high-voltage, wide pulse to the device but in normal use it acts as a read only cell.

The requirement for read/write memory has been met primarily by core memory with some applications utilising plated wire. Core memory has a long history of reliable operation and is used in many airborne and space applications. Compared to semiconductor memories it suffers from greater volume and more demanding power supply requirements. There is also an integrity problem as the information in a core memory is destroyed every time it is read and must be restored.

This problem does not exist with plated wire memory. The reason for plated wire memory not becoming more popular is due to the difficulty in manufacture of the plated wire and the large investment in development required. Where it has been used however, results have been very satisfactory as it has all the characteristics previously mentioned as desirable in an airborne system.

8.2.6 System Configurations

There are two differing approaches to the use of digital computers in airborne systems which have become known as the integrated and federated approaches. The federated approach is for each aircraft sub-system to contain a processor and memory tailored to the requirements of that sub-system and not necessarily having any commonality with other systems. The integrated approach calls for a small number, possibly one plus redundancy, of computers centrally available to perform computing tasks for sub-systems. There is no single optimum solution to the problem, very much is dependent upon the particular system. Advantages claimed for an integrated system are reduced weight and costs and improvements in performance, reliability and maintainability. A problem with an integrated system however is in the management and co-ordination of the various systems[1].

A compromise solution which has been proposed is a modular processor and memory, each system using the same hardware, as required, as well as communicating with a central processor where some common, and possibly non-flight safety essential, tasks could be carried out. This approach obviously alleviates the maintainability and software problems.

8.2.7 Software

An airborne digital system must be provided with software which will operate reliably, and functionally to specification, in the airborne environment.

The first decision is the type of programming language to be used in the machine, the two extremes being a high level language, such as FORTRAN or CORAL, and the other machine code or assembler language. The advantages of a high level language are the independence, to a degree, of the software from the actual hardware used and the higher productivity obtained from a programmer. Thus it is possible to compile a CORAL programme to run on any airborne machine whereas one written in the assembler language of one machine is not usually convertible to a different machine. The second point is that, given a problem definition, a programmer can produce a debugged program in CORAL in a much shorter time than in assembler language.

Against these advantages are the costs associated with using high level languages. Not many airborne computers have high level compilers available for them whereas most machines have assemblers. The provision of such a compiler can be a time-consuming and expensive task. The final machine code produced by a compiler will require more storage space, and will take longer to execute, than an optimised machine code programme. Therefore where time, and/or space, are at a premium, assembler language programming will provide the programmer with the means to produce an optimum solution. This is often the case in airborne real-time systems where permissible execution rate may be determined by the dynamics of some aircraft system. This time minimisation can not be achieved if a high level language is being used.

The cost of computer processors is falling such that in future it will not form a significant item in a total digital system. A much larger cost share will be attributable to the memory. There is therefore, incentive to minimise the

amount of memory needed particularly if production runs of the equipment are required. This again can best be achieved with assembler language programming.

A comprehensive solution may be the method described earlier of implementing "high level" instructions in hardware. This approach is only economically feasible now that microprogrammed processors are available.

An important aspect of software is the reliability that may be expected. This may be overlooked when considering total system reliability but it can be an important contributor particularly in large systems. Experience shows that the number of software faults is very dependent upon total program size, thus where 1 fault may be expected in 1k words of machine code, the number would be near to 100 in 10k words. The usual approach, which appears in many guises, is to modularise the software. The software is broken down into a number of definable modules which are un-ambiguously specified. Each module may then be tested and debugged in isolation so that the final system is comprised of proven modules.

It is very important in airborne systems, particularly those which involve aircraft safety, that software is subjected to similar controls, standards and modification procedures as are applied to airborne hardware.

8.3 APPLICATION TO AIRBORNE SYSTEMS

It is possible to identify two diversions in the application of digital computers to airborne systems[2]. These are real-time situations, such as the processing of radar or communications data, or the control of a system, and data-processing operations, such as in AWACS, (Airborne Warning and Control System). In the real-time situation the computer is a system component and is usually ancillary to the primary function whereas in the data-processing system the computer and peripherals are the system and the computing task is an end in itself. These two divisions each place their own requirements on a digital processor and can result in very different hardware and software implementations.

A number of applications are now described which are typical of present day airborne digital systems.

8.3.1 Fuel Management

A problem in larger aircraft with multiple fuel tanks is the management of the quantity of fuel in each tank in order to maintain trim and centre of gravity requirements. This problem is exacerbated with military aircraft where stores are disposed of during flight.

The problem has been solved manually with a flight engineer transferring fuel when necessary to maintain the trim and CG requirements. The USAF/Rockwell B-1 utilises a digital computer based system which continuously monitors a number of parameters and controls the necessary fuel valves. Among the inputs considered are fuel tank sensors, flap and wing position, altitude, pitch and roll rate, landing gear position and Mach number. The outputs provided are fuel quantity information to the crew and control of all fuel transfer activities.

The system also interfaces with the stores management system to prevent any stores unloading from compromising the CG limits and to schedule order and rate of stores unloading.

The processor which is duplicated, uses large scale MOS integrated circuits.

8.3.2 Engine Control

Engine control systems currently in production and in advanced state of development fall into two main categories. The first consists of those with predominantly hydromechanical components with limited engine mounted electronic analogue trimming controls to cater for such functions as temperature and speed limiting.

In the second category are those engines such as the RB.199 with full authority duplicated electronic analogue controls, where only limited flight experience is available in comparison.

The hydromechanical controls are based on mechanical devices and a typical control can achieve defect rates of less than 0.1 per thousand hours.

Analogue electronic systems reliability data is available where a defect rate of less than .05 per thousand hours is being achieved.

Figures such as the above set targets for digital controls, and it is against these that the system integrity must be gauged. It may be argued that already having two technologies there is little need to embark on a new one, but three factors militate against this.

- Both hydromechanical and analogue electronic controls attempt to achieve complex requirements but usually on the basis of a specific application. This implies that a new set of development costs is incurred for each application.

- There is physical limitation to the degree of complexity that can be built into hydromechanical and analogue controls. For example both systems find it difficult to deal with multi-function generation and reliability drops considerably as the computing requirement is increased.

- In general it has been the custom to have independent control systems for main engine, reheat, nozzle and variable intake. Little opprotunity has been taken to integrate any of these functions, but as power plants become more complex there is a need for this to be done.

For these reasons digital computers are now becoming the accepted method of controlling sophisticated gas turbine engines that is, where intake, main engine, reheat and nozzle systems are involved.

A typical system[5] consists of a ½ ATR long case containing a general purpose digital computer together with the necessary input and output conversion electronics for the various transducers and the system power supplies.

The computer architecture is of an advanced concept, including features such as multiple registers, microprogramming, and overlap and pipelining of instructions. The system contains a core memory of one microsecond cycle time, but the processor design allows an instruction rate of up to 5 MHz to be achieved. The word length of the instructions and data words is 16 bits, although the required control accuracy of 0.1% requires only 10 bits of information. To achieve 10 bit accuracy, the input conversions are designed for 12 bits and these 12 bit data words are input to the computer. Although they could be handled in a 12 bit computer, the computations are eased in a 16 bit machine. This 16 bit word length also gives the possibility of an increased number of instructions and flexibility of addressing.

The computer is designed to operate in an ambient temperature of up to 75° while consuming 80 watts of power. Under these conditions the MTBF is estimated at 3500 hours.

The computing power of this processor is sufficient for any modern powerplant, dry engine and reheat control, together with some spare capacity. Two factors are of importance in estimating a computer requirement: — the speed of operation and the range of computations possible, although they can be traded off against each other. A primary requirement for this system is the ability to react in a fault condition to freeze the actuators before they can "run away".

The memory used in this system is a core memory of nominal cycle time one microsecond. For development exercises core memory has a number of advantages; it is non volatile, electrically alterable and it is available. As core memory is read/write, the program may be changed in situ for the incorporation of modifications, and any portion of the memory made available to the processor to use as workspace.

8.3.3 Flight Control

A considerable amount of development work is taking place in electrical signalling of control surface demands in both fixed wiring aircraft and in helicopters. There are advantages to be gained from the replacement of rods and links with electrical connections:

- Greater design freedom in routing,
- Improved positional accuracy,
- Improved handling through optimised control interlinks,
- Improved failure survival.

The incorporation of a digital computer into the system has resulted from the development of aircraft where conventional aerodynamic compromises have been improved by the use of an automatic control system which maintains basic stability. These techniques are known as "Active Control Technology", or ACT, and a vehicle so designed as a Control configured Vehicle or CCV. The only true CCV aircraft i.e. one which has been designed from its conception as being totally unflyable without sophisticated automatic control, is the General Dynamics YF16.

There are other aircraft flying with a "pseudo" fly-by-wire in which the electrical signalling system is backed up by a mechanical system e.g. MRCA and Concorde. The only aircraft flying without this mechanical back-up are the F8. YF16 and a Chinook helicopter which is being used as part of the Boeing heavy lift helicopter programme.

A development programme has been carried out with an F-8 aircraft using hardware from the Apollo guidance, navigation and control systems[3,4]. The computer used was a 16 bit fixed point machine with a 36,864 word read-only memory and a 2048 word scratch-pad memory. For this type of application a longer word length would prove more suitable together with floating point operation. Both of these features are more readily available today than when the above systems were conceived.

A major problem in these systems is the system reliability required. This reflects both on the hardware and on the software design and management. Hardware reliability figures in the range of 10^{-7} to 10^{-9} failures per hour are required and these can now be achieved by the use of multiple redundancy, that is the use of several control lanes in parallel with a degree of cross examination and in some systems self-correction.

8.3.4 Data Collection

Under this heading are systems where the primary intention is to acquire data and then carry out computation followed by some permanent record.

Early examples of these systems were AIDS, Aircraft Integrated Data Systems, which did not contain a computer, data was input, converted to a digital format and stored on wire or magnetic tape. A development of these systems has been the incorporation of a computer to perform some processing of data, either to allow conclusions to be drawn in flight or to reduce the amount of data stored for subsequent ground analysis.

An example of such a system is one for monitoring the state of a gas turbine engine. Various engine parameters are input to the computer: pressures, temperatures, vibration levels, shaft speeds etc., and these are used to estimate the degree of wear or life remaining for different components of the engine. Turbine blades, for example, have a life which is a function of speed and temperature. The computer is used to compute this integral, also allowing for other secondary effects, and to keep an updated measure of turbine blade life. A suitable read out is provided for ground engineering staff.

More complex systems carry out trending of data, where, by extrapolation, conclusions are drawn about the time before a computed parameter reaches a pre-determined limit. This system permits overhaul to be scheduled when required by the engine condition rather than after a fixed time interval.

8.3.5 Electronic Counter Measures

ECM systems have been in use for over thirty years, but in the last fifteen years have come to rely heavily on general purpose digital computers. The first application was in the processing of radar signals where the computer was used to identify signals in the presence of both natural and jamming interference.

A primary area of use today is in power management. The computer identifies the various signals requiring to be jammed and makes decisions as to the apportionment of the system resources, frequency, power, antennae etc., between the various threats. The system may be also, making use of previously obtained information, identify the radar sites in question and programme the counter measures based on the known parameters of that radar source.

The requirements for the processor in ECM systems are high speed data input ability and computation and instruction sets with certain ECM-type instructions.

The speed requirements are determined by the necessity for the system to work in real-time, inputting pulses as they arrive. The rates involved make programmed input to the computer impracticable and direct memory access (DMA) must be used. Computers designed for these systems have DMA input rates of up to 10 million words/second. The majority of processors used are 16 bit although some 24 bit designs have been used. To speed up the processor instruction rate various features are used, two common ones being multiple accumulators, up to 16, and pipe lining of data and instructions from memory.

The memories used are usually semiconductor, ROM, PROM and RAM and a typical system may have 8–32k words.

8.3.6 Airborne Warning and Control System (AWACS)

The AWACS computer system is one of the most complex single computing systems in airborne operation at this time. The function of the system is to monitor inputs from a wide range of sources – communications, radar, operators etc., to maintain a data base for the mission and to calculate navigation parameters, guidance data, the status of weapons and other such tactical information.

The computer system comprises duplicated processors and a number of core memory systems. This computing capability is supported by magnetic tape and drum mass storage, a line printer, punched taped and operator console. Communication with other aircraft systems uses two input-output busses designed for high speed operation. The redundancy of peripherals, processors, memories and input-output facilities provides a high degree of system integrity in the fault case and very fast, powerful computing ability in normal operation.

The speed of operation of the processor is achieved with the following techniques.

- Use of a cache memory between the processors and the main core memory.
- Multiple sets of general registers to enable switching of tasks without saving, and subsequently restoring, all registers.
- Use of Schottky logic in the design.
- Microprogrammed instruction set in ROM memory.
- Instruction overlapping.
- Multi-address instructions.
- Large instruction repertoire (174) including both fixed and floating point instructions.

The system software is written in JOVIAL, the USAF standard language for command and control systems. Apart from the necessary operating software the system includes both pre-flight and in-flight diagnostic programmes, training software and programme generation packages.

8.4 CONCLUSIONS

Digital systems do not yet provide a technically acceptable and economic solution in all areas in which they have been used. Further, digital control does not provide an automatic panacea for system problems evident in more traditional technologies. If a decision is reached to utilise a digital computer in an airborne system then full consideration must be given to a number of factors:

- Life cycle costs,
- Unit reliability,
- System integrity,
- Maintainability,
- Software.

The cost problem must be evaluated on a life cycle basis. This is obviously true for any system procurement, however digital systems tend to appear less economic if only acquisition costs are considered. As a major benefit of digital systems is the much reduced time and cost involved in modification, then a total cost-of-ownership evaluation must be performed.

A distinction has been made between reliability and integrity. The reliability refers to the rate at which a particular unit will develop a fault and require repair. The integrity of the complete system is a measure of its ability to continue performing to specification in the event of one or more faults occurring. Thus it is possible to design a system with high integrity obtained through a multiplicity of unreliable units as against a single highly reliable unit. Every design is of necessity a compromise and the reliability and integrity requirements vary considerably according to the role of the aircraft type in question and the system concerned.

Potential problems with software have been mentioned earlier, the decision as to type of programming to be used, the design of the software system and the control of this design and subsequent use. With these and similar problems resolved, software can provide the means whereby the flexibility inherent in a digital solution may be fully exploited.

It is anticipated that the use of digital computers in the airborne situation will increase considerably in the next decade, with the development emphasis moving away from innovation and sophistication towards standardisation and commonality of equipment.

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REFERENCES

1. Bentz, C.E. — *The Role of Computers in Future Propulsion Controls*. AGARD Conference on Power Plant Controls for Aero-Gas Turbine Engines, AGARD-CP-151, 1975.

2. Eccles, E.S. — *Airborne Computer Systems*. Smiths Industries Limited in private communication to the Working Group.

3. Fraser, D.C. Felleman, P.G. — *Digital Fly-by-Wire*. Astronautics and Aeronautics, July/August 1974.

4. Szalai, K.J. Deets, D.A. — *F-8 Digital Fly-by-Wire Flight Test Results*. Flight Mechanics Panel Sympsoium on impact of Active Controls Technology on Airplane Design, Paris, 1974.

5. Powell, R.D. Griffiths, D.M. — *The use of Digital Control for Complex Power Plant Management*. AGARD-CP-151. Power Plant Controls for Aero-Gas Turbine Engines, 1975.

CHAPTER 9

SUMMARY AND RECOMMENDATIONS

by

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9.0 The preceding presentations have served to manifest an overall coverage of the current and near future major technical thrusts in the digital data processing area and are indicative of the state-of-the-art in particular disciplines. The impact and the exploitation of these new possibilities for application to the NATO Military environment will give rise to improved reliability, effectiveness and related economies. In the comments that follow each chapter has been reviewed and a technical appraisal has been made which will attempt to match current technology attributes to the tactical military situation. Wherever possible commentary is offerred which might enhance the subject area of each chapter so that as broad a coverage as possible is given to this particular subject area. Additionally so as not to misrepresent the state-of-the-art as a panacea for all problems that may arise from satisfying the requirements of the NATO military environment limitations of each technology are noted when applicable.

9.1 The absolute reduction in size, weight and power, for a given performance (speed and reliability) allows the use of the newer digital devices in defensive and offensive missiles, satellites, vehicles, and man-pack applications. Undetectable sensors and processing elements can be used in field operations, based on the new technologies. During the period of the 1960s and 1970s, the evolution of electronic circuitry has come from the discrete components to the highly complex integrated structures. This evolution began with the bipolar family of devices and quickly developed into the DTL, RTL, TTL and ECL logic families, each providing some contribution in the areas of speed, lower power consumption or levels of integration. Later, refinements to these technologies produced TTL-Schottky, low power TTL and high threshold TTL.

More recently introduced, the MOS family of devices has found widespread application. As with bipolar devices, MOS development began with the discrete transistor and evolved through the development of various materials and processes into logic families. Production improvements also allowed the level of integration to increase.

Several factors enter into the selection of the basic technology used for a particular application. In the tactical military environment, the primary parameters involved are reliability, power consumption, and speed, with integration level, cost and the ability to construct complex circuits (fan out) also being taken into account.

Thus, the rapid evolvement of elements relating directly to computer technology has made it realistic to use the computer in many more aspects of the Command and Control Problem, especially in the tactical field and in airborne stations (e.g., AWACS, Airborne Command Post).

The use of the newer technologies in data processing (such as computers, minicomputers, microprocessors, etc.) in tactical Command and Control Systems allow the commander to have the latest military information at his disposal in readily assimilated form and will permit different strategies, options, etc. to be explored prior to execution of orders. This should increase the accuracy and timeliness of these orders.

Today, the use of digital techniques has improved the reliability and reduced the cost of hardware components that are used to build data processing systems that are embedded in tactical command and control systems. These techniques have also enabled systems to be designed and implemented on modular and higher levels than the gate and circuit level of previous systems. These new design approaches have reduced the design and implementation cycle for hardware. In addition, both hardware and software failures are easier to detect and repair.

9.2 Since military computers, specifically those in a tactical environment are often called upon to perform under stringent operational conditions, far greater than the standard environments, it follows that packaging and assembly techniques must be the most reliable and the most efficient schemes available. The evolution of computer generations has resulted in a continuous reduction in size, and power consumption, as well as an increased speed of operation and reliability.

Integrated circuit (and LSI) usage is becoming more prevalent with IC's being used to perform many logic functions, and also as data storage units. New types of integrated circuitry have the promise of extremely high density, high speed of operations, and low power consumption [i.e. CMOS-SOS (complementary metal-oxide-silicon) (silicon on sapphire) devices].

In order to fully exploit these new types of integrated circuitry for the tactical military environment, many trade-offs must be considered in addition to those which arise as the technology develops. Preliminary and on-line testing techniques must be considered, as well as the effects of standardization. Repair and routine maintenance must be considered in this special environment since reliability could affect the success of a particular mission.

As a design tool, packaging levels are usually arbitrarily assigned. The levels usually considered in the packaging design are the basic circuit level, the functional module level, the LRU level and the total equipment level. In a specific tactical system, levels may vary as computer designs vary, but for planning purposes, the above are generally the most useful. Design configuration must, to the maximum extent possible, be planned to facilitate the sequence of maintenance procedures (testing, fault isolation, disassembly, replacement, alignment, etc.) to eliminate redundant operation, or awkward activity.

Interconnections, both within a level, and between levels, are probably the most important technical factors. Again, the packaging engineer must determine the most reliable, least costly and most efficient method for connecting the basic circuits, the functional modules and the LRU's so that total computer performance is optimized. Repairable vs throw-away modules at all levels must be considered from a logistics standpoint. Module reliability and cost usually determine whether a module should be discarded or repaired.

The environment the computer must live in also determines how it is packaged. Vast differences exist between the techniques for packaging tactical systems and packaging large processing units in controlled environment fixed based systems. The packaging designer must be fully cognizant of all environmental constraints prior to beginning his design.

9.3.1 Core memory has served well for Command and Control tactical applications. However, cost and size problems have been a limiting factor on the quality of main memory used with tactical systems. The advent of large, cheap semiconductor memories gives promise of significant cost and size savings in tactical systems, as well as permitting higher speed operation of the computer. The use of large semiconductor memories in tactical computers can significantly reduce programming costs and improve system response time.

Bubble and CCD technology will slowly lead to the replacement of mechanical mass storage with electronic devices. Ultimate application within the near future will insure that economical fast storage for large data bases will become available for tactical use. This will foster widespread use of data management in tactical environments. Those Command and Control System functions not presently feasible in tactical systems will now be practical.

Extremely large memories for retention of data from Command and Control exercises, recording input data, etc. required for organizing storage and retrieval systems associated with tactical Command and Control, tactical intelligence processing systems, and for sensor processing systems still require additional efforts in development.

9.3.2 **Microprocessors** will have a profound impact on all forms of tactical systems. The availability of low cost processing capability will lead to the distribution of computational and control functions among many cooperating processors. This will enhance the serviceability and reliability of the total system. The microprocessor will permit the incorporation of intelligence into many functions and tasks where only simple logic was previously permitted.

The advent of the microprocessor will place an increasing burden on communications within and between system elements. While the microprocessor will allow data reduction to be done in many cases at the source of the data, this improved means of collecting will mean that more information will be passed within the system. The cooperating microprocessor complexes will require complex interprocessor protocols and intelligent switching devices to pass data and control between members of the complex. Additionally, they will ease system integration and reduce software complexity. These devices have not received wide range militarization to date; but there does not appear to be any technical barriers hindering such application.

9.3.3 Significant potential for tactical data systems exists in the development of computer system architecture. The performance of a computer system, out of necessity, depends largely on the coupling between the related subsystems which are matched to each other by interfacing them. The interface main tasks are:

- Matching of data rates.
- Matching of electrical characteristics.
- Supply of unique control signals for each subsystem.

Various computer systems built with novel architectures are in development. For example, a major effort is the Common Family Architecture (CFA). The approach being used is to select, validate, and specify an existing family architecture as the basis for the development of a software compatible family of tactical computers. This concept still

allows the implementation to have different physical, electrical and performance characteristics but will minimize the proliferation and the software base problem. Software compatibility is achieved by the adoption of one machine or computer family architecture. Standardization of a computer family architecture will permit different platform requirements to be satisfied but will still allow the military to utilize all the common software developed for common family. It is apparent that this technology will have a profound impact on tactical command and control systems.

9.4 One of the current tactical computer system problems is characterized by the use of third generation technology which has an impact system size, weight, and power. The net result of this and related problems is that computers cannot be employed as fully and freely as needed in varied tactical systems as permitted by rapidly advancing technology. The objectives in interfacing are to maximize performance on both sides of the interface while minimizing the overhead across it.

In the tactical military environment the problems associated with the interconnection of processing equipments gives rise to two situations, namely; equipment whose application or environment requires custom construction and equipment which is part of a manufacturer's standard product line and can be used "off-the-shelf".

Integration of the components in the former situation is simplified by the fact that the interfacing design can be done concurrently with the basic equipment. Penalties of cost and development time become evident although they are not necessarily the result of the interface requirement.

Such is not the case in the latter situation. Equipment development time disappears and costs are reduced. However, should there be a need to interconnect equipments from different manufacturers, there can be errors in data widths, transfer rates and control information. Currently, some of these problems are being alleviated for parallel data transfer by the introduction of "black box" general purpose interfaces. These provide the system communication facilities for the data signals and minimum necessary control lines to the "outside world". Unfortunately, there is not currently available (and not likely in the near future) any wide spread acceptance of a standard for parallel interfacing which might benefit the military tactical environment.

With the general acceptance of the CCIT and EIA standards, bit serial communication appears to be a simpler matter.

A most noteworthy development which has improved the interface problem area is the introduction of large scale integration. The UART has reduced most parallel to serial conversion requirements to a single chip solution while the microprocessor has permitted the introduction of low cost "intelligence for both parallel and serial interface devices". It is easy to forecast that with the steady advances in the microprocessor technology many of the problem areas, particularly computer interface, of the tactical environment will be readily solved.

However, as stated in Chapter 4, until standards can be defined, accepted and adopted, interfacing will remain as the production of unique solutions to unique problems.

9.5 The requirement for communication between organizations is not novel; however, computer to computer communications on a widely distributed geographic scale has been in existance only since the late 60's. The application of computer technology to the communications field has increased possibilities in the area of inter human communication and has made possible effective inter computer communication. The use of digital computers in Military Tactical Systems, and, in general, in Command and Control Systems is dictated by the necessity to increase the effectiveness of human control capabilities, i.e., to reduce the manhours spent in filing, retrieving and processing information. Since Command and Control Systems, which contain many functional subsytems, have to communicate with each other along and across the line of command, the problem of the integration of data processing equipment arises.

Within the tactical environment, information can be transferred via network from various field sites to processors for analysis then to command units or weapons centers. The present advances in computer and communications technology has made the comprehensive near real time command and control system possible. The upgrading of existing command and control systems to provide greater flexibility, speed and coordination of a greater number of information sources will continue to the mid 80's. Thus, a capability is provided for the concept of a military network which can deliver any type of traffic in accordance with operational military requirements, such as responsiveness, security, mobility, flexibility, reliability, surviveability, ease of operation, and ease of maintenance. All these characteristics must be provided using very flexible equipment which can perform logical, computational, control and buffering functions without requiring human intervention for the allocation of resources to the actual operational needs, and which can be used according to several assembly schemes to implement various network configurations.

In a military organization with a large number of computer centers, computer networks offer the possibility of utilizing existing resources to a greater degree. This can be accomplished if these centers were connected by a network. Centers which have reached their limits in processing capacity could send tasks to under utilized centers. Also, software which is available on a network could be used remotely without having to provide costly software conversion at the user site.

It has been shown that by executing a task on a processor designed to perform that task, that advantage can be obtained in cost and speed by factors of 10 to 100 over a generalized computer facility which is able to perform many tasks. In this instance, specific processing tasks would be transferred to specialized processors on a network rather than maintain a generalized computer facility.

Another promise of computer networks is the ability to produce a dynamic facility. That is the user of a military network could logically compose a set of resources from the available resources which he would use to concentrate on his current processing problem. As his problem changes, a new set of network resources can be orchestrated. In this case, the user would view the network as if it were one machine and not a diverse collection of computer centers located at various military installations. In order to produce this transparency of the network, a system must be interfaced between the user and the network. This system which manages the resources of the network and makes the network a convenient tool for the user is called a Network Operating System. Work on developing network operating systems will proceed over the next decade and promises to make a network an extremely sophisticated processing system.

In the final analysis of networking, applications to the tactical military system digital computers are consistent with the adoption of digital techniques for the transmission of voice and data for circuit and message switching, as well as for modulation and multiplexing. Potentially, computer networking promises the fulfillment of the aforementioned functions with significant economies where ever information processing is required.

9.6 The rapid evolvement of computer technology has made it realistic to utilize the computer in many more applications of the military situation especially in the tactical field and in airborne stations (e.g., TACS, AWACS, Airborne Command Post). Large scale application of digital techniques in the signal processing area alone represents a significant advance. This total technology is ready to be applied to a much greater extent to the Tactical Command and Control Systems. In order to further exploit this rapidly progressing technology, additional developments must be carried out to make this transition.

To date, major inroads of digital techniques have been made in signal processing which is an essential element of surveillance, guidance, fire control and other systems requiring the processing of signals collected by sensors before the information can serve a useful decision or control function.

The major impact of the emerging digital technology is in cost, performance, flexibility and adaptability, and total integrated system. Digital systems are more cost effective than analogue technology. This is becoming more profound with present advances in the logic and memory integrated circuit technology. These technologies provide across the board improvements in cost and performance, so that more complex structures can be implemented at a smaller cost. This permits developments which are occurring rapidly, of devices that have increased computational precision and allow the implementation of algorithms that previously were awkward or impossible to implement.

Besides the practical cost implications of initial system implementation, digital technology allows the implementation of systems that offer great flexibility and adaptability to a wider variety of system parameters and changes in them. This has become a reality in recent years due to the maturing of the microprogramming and the microprocessor technology.

Progress in the digital technology makes possible the developments of "total integrated command, control and communications systems" for use in a tactical environment. The technology is here. The benefits that are currently being reaped are the result of progress in the general purpose digital computer technology. This progress has been due to advances in device technology; however, advances in computer architecture based on the availability of cost-effective hardware are playing an increasing role. To overcome performance limitations of the traditional serial computer system, parallel/concurrent processing systems are being developed. This technology is still in the early stages of development. The pacing item is user oriented software to make use of the power of these concurrent processing systems. Some are in operational use, others are experimental in nature and used in development programs. Application analysis, algorithm development and computer architecture studies must be conducted by the NATO Military Organizations to apply this developing digital technology. To be useful in tactical situations, militarized hardware must also be developed. This will probably be a somewhat pacing item since current parallel computing systems operate only in the typical "computer center" environment.

While a continuing era of rapid development will be anticipated in the digital signal processor area (related similarities of hardware components and requirements for general purpose digital computers), it is reiterated that programming of the computer process has not kept pace. High performance digital signal processors and their applications have thus been limited in their deployment in Command and Control computer systems.

9.7 Traditionally, most research and development of tactical data handling techniques has been addressed to ground-based equipment. The continued pursuance of this concept could seriously degrade some of the operational capabilities of future tactical aircraft. In order to circumvent this situation for current and planned generations of tactical aircraft, it is mandatory that the development of future data handling techniques be based on a more complete set of requirements; specifically, both a ground and an aircraft environment.

Basically, those aircraft using extensive data handling systems have a common problem: how to extract useful information from the large mass of data collected by the airborne tactical system sensors.

Aside from stringent physical requirements (volume, shape and weight) and environmental requirements (temperature and pressure) the problem of reliability must also be addressed. Final design therefore involves a number of tradeoffs which are germane to particular requirements of the tactical airborne situation.

Contemporary airborne computers have been oriented towards specialized instruction sets and with the advent of semiconductor memories, the field is ripe for microprogrammable processors. Conventionally, a microprogrammed processor offers the same processor hardware be provided with different instruction sets assigned to different applications.

As with its companion ground equipment, the tactical airborne processor has been impacted by the use of higher speed logic devices and the development of processor architectures (increase in paths of parallel operations increases speed).

The optimum solution to a suitable memory (e.g. read only, but electrically reprogrammable, non-volatile, nondestructive readout) has not been reached in the airborne system. Semiconductor memories are, however, rapidly becoming available to meet these requirements.

Dependent on the application, the use of digital computers in airborne systems is somewhat different in system configuration. Those aircraft requiring the most extensive use of data handling systems are: Attack, Special Electronic (ECM), Airborne Early Warning Radar, Surveillance and Anti-submarine. Each application has no single optimum solution to the problem even though each integrated system is potentially designed for reduced weight and costs and improvements in performance, reliability and maintainability.

Presently, major development efforts are underway to develop a software compatible family of tactical computers and associated systems/support software. One such effort is the Digital Avionics Information System (DAIS) which is a major USAF effort to standardize future USAF aircraft avionics computer systems. The overall effort includes the processor and its highly reliable quadruplex bus input/output system, programming support and hot bench test capabilities. The programming support system provides a HOL language capability, a system design and verification (SDVS) subsystem for developing the avionics operational software on a simulation input/output basis and on a hot bench basis.

It is most likely that the technologies relative to the current NATO/Military Tactical environment will be used in computer systems in the 1980's. Without a doubt their capabilities will be steadily improved over the next decade or so until approximately the 1990's when they approach a point where fundamental physical laws governing the device characteristics of their manufacturing processes will prevent further improvements. The systems engineer concerned with the military tactical environment faces a major task in order to determine credible theoretical and practical performance limits of components, circuits, and subsystems and make application to such an environment. He must be prepared to match available technologies with new trends which may be detected in the requirements for data processing systems operating at tactical ground-based or airborne facilities. In summary these current and near future trends (1980's) call for computer systems designed to:

(1) Withstanding demanding environmental conditions (including nuclear effects).

(2) Have high reliability and on-line maintainability.

(3) Satisfy the size-weight-power constraints.

(4) Provide data security.

(5) Be capable of relatively high data-processing rates.

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14. Abstract

New developments in solid state technology have emerged which make possible significant improvements in computer capability. These improvements allow for wider applicability of data processing equipments in effecting command and control in the NATO military environment.

Solid state technology has decreased by orders of magnitude the volume and power required by computer circuitry and hence has made possible more sophisticated data processing. The technology is now available to construct high level language computers; to control functions in hardware rather than software, to build microprocessors for distributed use in tactical environments; to make available for field use low power, non-mechanical, mass memory systems; to tailor computer architectures to specific applications, and for many other innovative uses.

This report sponsored by the Avionics Panel of AGARD, describes the solid state technical developments and assesses the importance of these developments in their application to satisfying NATO military requirements.

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Digital computers
Microminiaturization
Command and control
Military operations
Programming languages
Computer applications

AGARD Advisory Report No.100
Advisory Group for Aerospace Research and Development, NATO
COMPUTER APPLICATIONS
Editor: I.J.Gabelman
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